Interpret System Clock Functions

L61524

LCN

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This module supports **TotalPlant** Solution (TPS) system network.

TPS is the evolution of TDC 3000X.

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Table of Contents

Figures and Tables

Acronyms

CS/R	Clock Source Repeater
FOCT	Fiber-Optic Clock Receiver
FOCT	Fiber-Optic Clock Transmitter
HVTS	Hardware Verification Test System
LCNE	LCN Fiber-Optic Extender
LCNFL	LCN Fiber Link
RTOS	Realtime Network Operating System
SMCC	System Maintenance Control Center

Introduction

Module Overview

About this module

Each node on the LCN has an internal sense of time. Under normal operations, time is synchronized in all nodes. The mechanism by which this synchronization occurs depends on the processor types of the nodes on the LCN:

- a non-KxLCN system,
- an all KxLCN system, or
- a combination of both types of processors.

Objectives

Given a Universal Station or Global User Station (GUS) on an LCN that can access the diagnostic clock displays and the System Maintenance Control Center (SMCC), the student will be able to do the following:

- Determine the LCN clock configuration and clock status.
- Perform troubleshooting to determine the location of crossed LCN cables.

Interpret System Clock Functions

LCN Clock Management Concepts

Clock Management

LCN Clock Management is an RNOS software subsystem that is used to maintain the date and time in the node. It provides services to

- set the network time,
- read the network time,
- convert time formats,
- perform arithmetic operations on time, and
- handle the Watch Dog Timer.

System time formats

System time, existing in internal time format, may be converted from any one of three time formats to another:

- Internal,
- Gregorian, and
- Julian.

Internal time values may be added or subtracted.

Watch Dog Timer

The Watch Dog Timer is an independent hardware entity that, as one of its functions, checks the operation of Clock Management. Every 50 milliseconds, Clock Management services the Watch Dog Timer. The Watch Dog Timer checks to see that it has been serviced every 100 milliseconds.

Software Watch Dog Timer

The Software Watch Dog Timer is an RNOS timer used for infinite loop detection. The application software can set this timer to expire in some number of 50 millisecond ticks. The clock driver decrements the count on each clock interrupt and, if the count falls below zero, the node is killed. To prevent expiration, the Software Watchdog Timer must be either reset or disabled through the proper RNOS interfaces.

General Theory of LCN Clock Operation

Defining clock synch source

Under normal operations, time is synchronized in all nodes on the LCN through a digital message containing a count of the actual date and time.

There are two NCF-defined nodes that function as the source for LCN clock synchronization messages.

It is recommended that clock sources be nodes that are not often powered down, such as gateways.

Clock master/slave

Of the two NCF-defined nodes, the first node that is loaded becomes the clock master.

The second NCF-defined clock node that is loaded becomes the slave clock source.

The clock master periodically generates a clock message by which all other nodes on the LCN are synchronized.

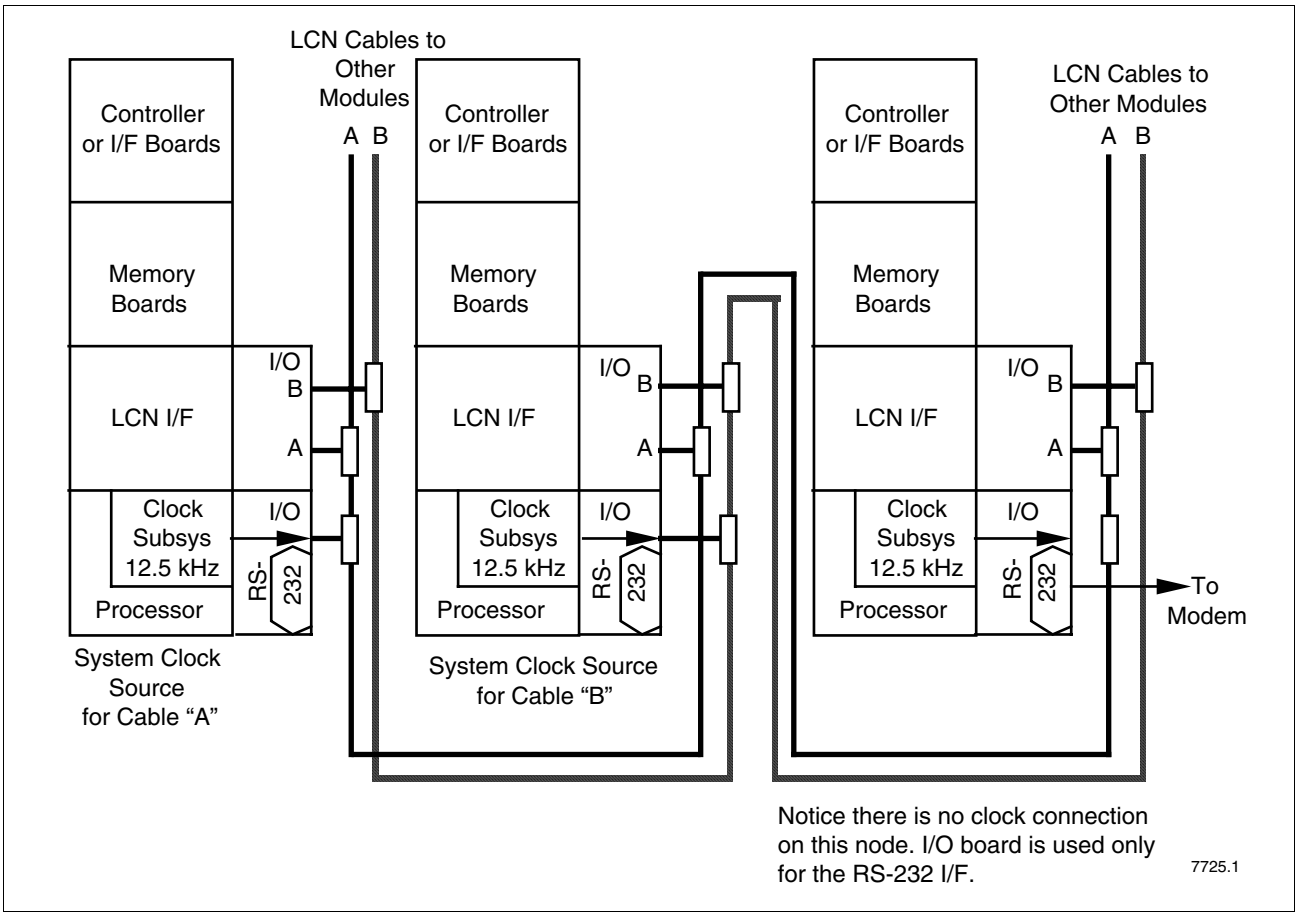


Figure 1 – System Clock Source

Remote segments

If the LCN has remote segments, the two NCF-defined clock sources must be located on the main segment; this is required to maintain synchronization with other remote segments in the event that one remote link fails.

The rest of the LCN (main and other remote segments) is unable to receive the clock synchronization message if the clock source nodes are located on a remote segment and the fiber optic connections to that remote segment fail.

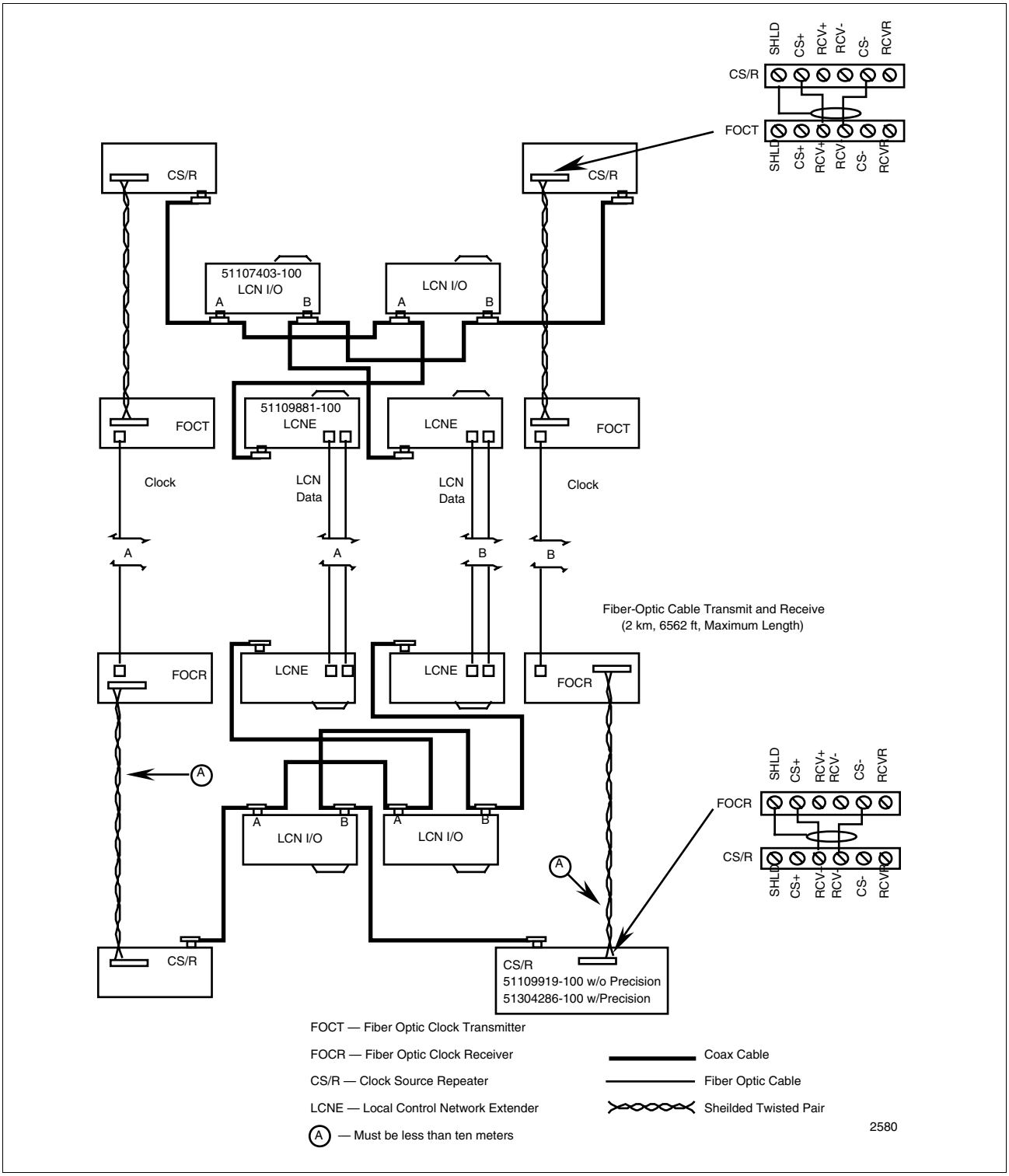


Figure 2 - LCN With Remote Segments

Synch process

Each LCN node's clock subsystem has its own internal sense of time. When a clock subsystem is told to synchronize itself to another clock subsystem

- First, it must adjust its internal sense of time to that of the synchronization source.
- From that point on, the clock subsystem monitors the clock source to determine if each newly received synch interrupt/time update is consistent with what is "expected:"
  - If the synch interrupt is within the margins allowed from the expected time, the internal sense of time is adjusted to the synchronization source time. (Non-KxLCN: 50 ms ±300 µs, KxLCN: 7 secs.)
  - Otherwise, no adjustment to internal sense of time is made.

All nodes that receive their time synchronization from the LCN broadcast are considered to be synchronized to the network.

Any node that is not the master or slave, and is expecting to receive a synch time update through the LCN, is considered to be in the "listener" clock mode.

Time keeping

In between time transmissions from the clock master or in the event that time is not broadcast through the LCN, each node keeps its own time. The update of this time is usually synchronized from the 50 or 60 Hz ac power source, although it could also come from an external frequency source.

When synchronization to the power line is initiated, no immediate adjustment to the internal sense of time is made. During the following cycles, the internal sense of time is adjusted as required by a small value (+/- 20 to 30 microseconds per 50 millisecond period) to maintain synchronization to the power line.

Local clock mode

Nodes that keep their own local time are not considered to be synchronized to the network. They are considered to be in the "local" clock mode. Assuming that the ac line power is clean and not subject to fluctuations, all nodes on the network in "local" clock mode should maintain time within a few seconds of each other.

Clock synch source

To specify whether a node will keep time from ac power or an external frequency source, the power supply in each node must be pinned for either internal or external.

Normally, all nodes are pinned for internal (line frequency) to keep time from ac power.

Table 1 – Power Supply Pinning

Pinning	Description
internal	If the power supply is pinned INTERNAL, the node is synchronized to the *ac power line frequency*.
external	If the power supply is pinned EXTERNAL, the node is synchronized to an *external clock source*.

ATTENTION

External pinning on the power supply disables the ac line synch.

UCN SOE time stamping

If time stamping of UCN Sequence of Events (SOE) is required, the master and slave nodes, as well as the NIM requiring SOE functionality, must be pinned *external*. The external source has a much more precise timebase than ac power and therefore affords better time resolution for event time stamping.

Clock failures

Listener nodes report a failure to receive the clock synch message frames only if the clock is not present on either cable A or B. If the clock is not seen on either cable, the detecting node initiates the "Investigate Suspect Clock" maintenance recommendation message to the System Maintenance Journal. Failures that cause the loss of a clock signal on one entire cable are reported against the clock source node only.

How time is initially set

The Node Administrator provides the capability to set the network time. Communication of network time is one of the Node Administrator's transactions. The sequence of events is as follows:

1. The user sets the date and time at a Universal Station or at a Global User Station.
2. The Node Administrator in that US/GUS immediately broadcasts the time change to all LCN nodes.
3. The master clock node, upon receipt of the Node Administrator broadcast, begins synching all other LCN nodes to this new date and time through its periodic digital time message.

Clock Operations in a Non-KxLCN System

Clock Hardware

The required clock hardware is

- a Clock Source/Repeater (CS/R) board, or
- a Precision Clock Source/Repeater (PCS/R) board.

The clock hardware must be installed in *I/O slot one* of a node containing an EMPU, HMPU, or HPK2 processor board.

Clock signal

In a non-KxLCN system, the LCN carries a 12.5 kbaud signal in addition to the 5 MBaud LCN communication signal. The 12.5 kbaud signal is generated by special clock hardware placed in the two NCF-defined LCN clock nodes.

The 12.5 kbaud signal carries a digital message containing a count of the actual date and time that is generated by the master clock node every 50 milliseconds. Each LCN node contains a receiver that can detect the 12.5 kbaud subcarrier signal and can interpret the digital clock message.

Remote LCN segments

Each coaxial cable segment, cable A and cable B, must have a CS/R board connection so that the clock message will be transmitted on each cable. For LCNs with remote LCN segments

- Clock nodes must be located on the main segment (see Figure 2).
- If the segments are more than 300 meters (but not more than 2 kilometers) apart from each other, additional hardware is needed to propagate the clock signal between the segments.
- If the segments are less than 300 meters apart, twisted-pair wires can be used to directly interconnect CS/Rs on the main and remote segments.

Remote hardware

Both LCN cables, A and B, require a set of hardware to propagate the clock signal on a remote segment:

- Each CS/R board on the main segment connects, with twisted-pair wires, to a fiber optic Clock Transmitter (FOCT) on the main segment.
- Each FOCT connects, through fiber optic cable, to a fiber optic Clock Receiver (FOCR) on the remote segment.
- The FOCR connects, through twisted pair wires, to a CS/R on the remote segment.

Single remote node

If a single remote node is connected to an LCN cable segment through an LCN fiber link (LCNFL), the 12.5 kbaud clock signal cannot be transmitted to that remote node. It will be in the local clock mode and will simply synch time from ac power.

Power supply pinning options

Normally, all nodes are pinned for internal (or line frequency) and keep time from ac power. If pinned for external, the external frequency source can be from

- a Precision CS/R board, or
- from a third-party precision oscillator.

Operations

Each node on the LCN listens alternately every 50 milliseconds on cable A and cable B for the clock message.

The master node transmits the clock message on its cable.

The slave node

- receives the message from the master as it alternates to the master node's cable,
- adjusts its clock message to be in synch with the master, and
- retransmits the message out on its cable.

In this way, all nodes receive the master node's generated time synch message on both cables. These nodes are considered to be in the "subsynch" mode.

Clock failure

The slave node takes over as the master and begins generating the clock message if it either fails to hear from the master or receives three invalid messages from the master within a 1-second period.

Clock Operations in an All KxLCN System

Clock hardware

Because the clock messages are transmitted at 5 Mbaud, the CS/R boards (transmitting at 12.5 kbaud) are no longer needed in an LCN system comprised of all KxLCN nodes.

The two NCF-defined clock source nodes should be located on the main coaxial cable segment.

Clock signal

The KxLCN clock circuits have an operational mode known as the digital clock mode. In this mode, the digital clock synchronization messages are communicated like any other LCN message at 5 Mbaud. These messages are actually a special type of LCN diagnostic frame. One of the two NCF-defined clock source nodes generates this diagnostic time synch frame.

The master node transmits the system clock information on both cables A and B once per second.

Recall that LCN messages are transmitted on both cables, but each node listens on only the cable to which it is directed by the token.

Remote segments

Because the clock message is sent out as a regular LCN frame, remote LCN segments are able to receive the message across the LCN Extenders and fiber optic cables at the 5 Mbaud rate; consequently, the additional clock hardware that was previously required to transmit the 12.5 kbaud signal remotely (FOCTs, FOCRs, and associated cabling), is not required in an all KxLCN system.

Single remote node

A single remote node connected to an LCN cable segment through an LCNFL will be in time synchronization with the rest of the LCN because it receives the digital time synch message across the fiber optic cables.

Power supply pinning

Normally, all nodes are pinned for internal (or line frequency) and keep time from ac power. In the case of a KxLCN node, external pinning causes the node to use the on-board Precision Clock Oscillator (present on each KxLCN) for the clock source.

Operations

The first of the two NCF-defined clock nodes that is loaded with operating software becomes the master clock source.

The second configured clock source node becomes the slave clock source after it is loaded with operating software:

- It first listens for a clock of any type on the A and B cables.
- If it discovers that digital clock synchronization frames are present, indicating that the master clock source is present and operational, it uses the received clock synch message to synch its clock with the master clock source.

The slave clock source node will not transmit any special clock synchronization data messages while it continues to detect clock synch messages generated by the master clock source.

Clock failure

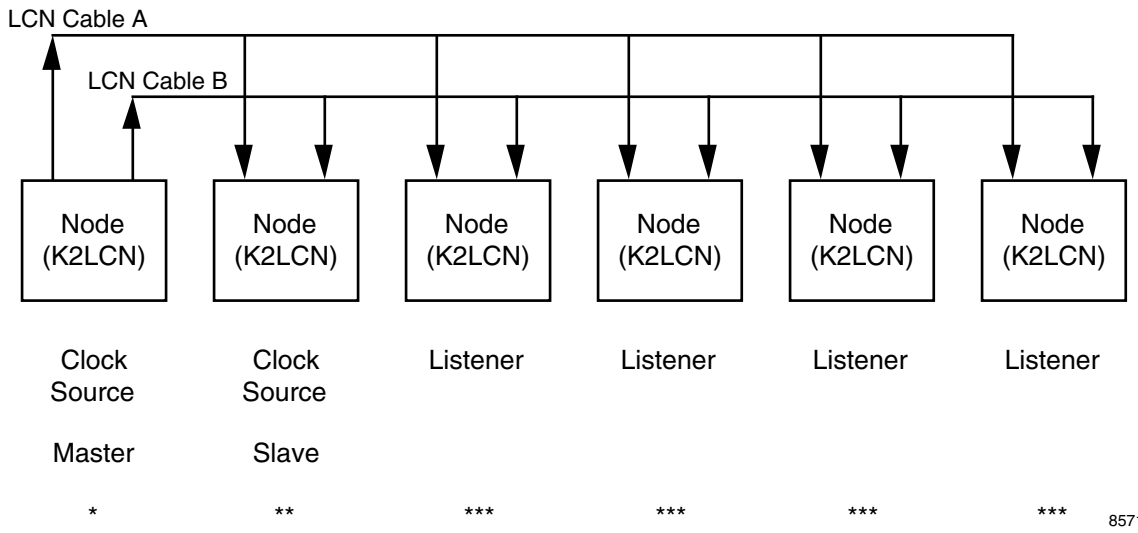
If the clock messages from the master clock source node stop for any reason

- The slave clock source node begins transmitting clock synchronization messages on both cables A and B between 7 and 14 seconds after the master fails.
- The slave clock source node declares itself as master.
  - If the original master clock source node is restarted, it first listens for clock messages. Once it detects them, it assumes the slave clock source responsibility.
- The remaining nodes (those nodes not configured as clock sources) become listeners in the "digsynch" or digital synchronization mode.
  - They detect the special clock synch data message and use it to synchronize their own clock circuits.

Example

The example in Figure 3 illustrates the digital clock concepts:

- The two leftmost nodes are configured as clock sources.
- The leftmost node was loaded first and is consequently defined as the master clock source.
- The slave clock source is second from the left.
- The remaining nodes are listeners in the digital node.



* = Once established as Master, listens to nobody. Generates clock sync message frames and transmits them on both cables A and B once per second.

** = Once established, listens for clock sync message frames on both cables A and B. Synchronizes its own clock using the received clock message frames from the Master clock source. Will transmit clock message frames only if the messages from the Master clock source stop. It will declare itself as Master clock source at this time.

*** = Listens for clock message frames on both cables A and B. Synchronizes its own clock with the Master clock source.

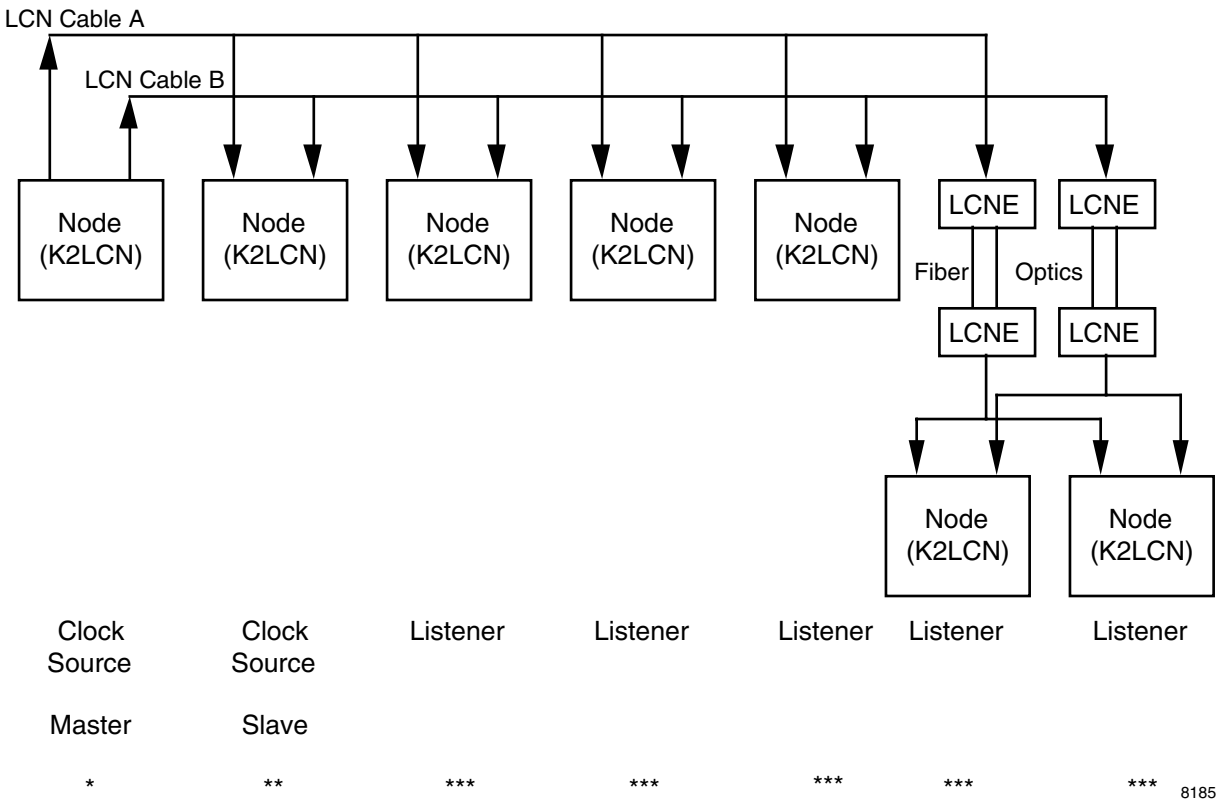
Figure 3 - All Digital Clock Mode System (Local Area Only

Remote segments

The example in Figure 4 illustrates the digital clock concepts when an all KxLCN system is implemented with remote LCN segments connected to the main segment through LCN extenders and fiber optic cables.

Figure 4 makes similar assumptions to those made in Figure 3.

In Figure 4, the clock message frames on the A and B cables are routed directly to the remote nodes through the fiber optic data link.



* = Once established as Master, listens to nobody. Generates clock sync message frames and transmits them on both cables A and B once per second.

** = Once established, listens for clock sync message frames on both cables A and B. Synchronizes its own clock using the received clock message frames from the Master clock source. Will transmit clock message frames only if the messages from the Master clock source stop. It will declare itself as Master clock source at this time.

*** = Listens for clock message frames on both cables A and B. Synchronizes its own clock with the Master clock source.

Figure 4 - All Digital Clock Mode System (Local and Remote)

Clock Operations in a Mixed System

Clock hardware

The two NCF-defined clock source nodes must be non-KxLCN nodes, because they contain the CS/R boards.

Clock signal—single LCN segment

LCN systems that include a mix of KxLCN and non-KxLCN processors require both the 12.5 kbaud and the 5 Mbaud clock messages.

As discussed before, the master node transmits the clock message on its cable at 12.5 kbaud. The slave node retransmits the message out on its cable. Each non-KxLCN node on the LCN, as well as the lowest numbered KxLCN node, listens alternately every 50 milliseconds on cable A and cable B for the clock message on the 12.5 kbaud subchannel.

Each KxLCN board has a clock mode (the subchannel clock mode) that is compatible with systems using Clock Source/Repeaters. When a KxLCN board operates in the subchannel clock mode, it can listen for and detect the 12.5 kbaud clock synchronization signal generated by the non-KxLCN master node; however, even though the KxLCN node can hear this signal, it cannot regenerate it.

Power supply pinning

Normally, all nodes are pinned for internal (line frequency) and keep time from ac power.

UCN SOE time stamping

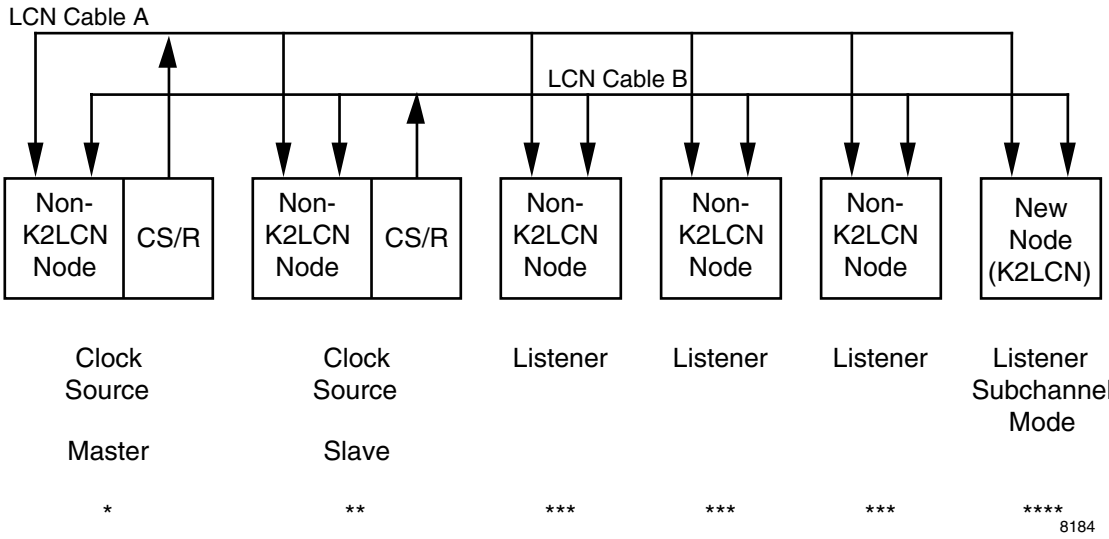
If external pinning is required for UCN Sequence of Events (SOE), the external frequency source for the master and slave clock nodes and a non-KxLCN NIM can be from a Precision CS/R board or from a third-party precision oscillator. If the NIM is a KxLCN, it receives its external synch signal from its on-board precision oscillator.

The sequence of events for a KxLCN node in a mixed system are as follows:

1. After it is loaded with operating software, the KxLCN listens for a digital clock synchronization message frame sent at 5 Mbaud.
2. If it does not detect a clock message at 5 Mbaud, it switches to the subchannel mode and checks for a 12.5 kbaud clock message.
3. Upon detecting the 12.5 kbaud message, it synchronizes its clock to the master clock source.
4. This node assumes there are other KxLCN nodes on the LCN, and therefore takes on a translator function. As a translator, it resends the received clock message frame at 5 Mbaud for any other KxLCN nodes that may be on the network. If there are no additional KxLCN nodes, the translation still occurs, but the translated message is not needed.
5. The translator is in the "subsynch" mode (it hears the 12.5 kbaud clock message); other KxLCNs are in the "digsynch" mode (they hear the 5 MHz clock message).

Example

Figure 5 illustrates the addition of a KxLCN node in an non-KxLCN system.



* = Provides the clock data to the CS/R board for transmission at the 12.5-kHz frequency on its cable. The clock is superimposed on the 5-MHz LCN signal on its cable. Once Master is established, it listens to nobody. It will assume the responsibility of Slave clock source when recovering from a failure.

** = Once Slave is established, it listens to the clock generated by the Master clock source, synchronizes its own clock, and provides the clock data to be transmitted by the CS/R board at the 12.5-kHz rate on its cable. It will continue to transmit the clock if the Master clock source fails. At this time, it declares itself as Master and listens to nobody.

*** = Listens for the 12.5-kHz clock on cables A and B.

**** = First listens to both cables for a digital clock sync message frame. If none is detected, it listens for the 12.5-kHz clock signal. If a 12.5-kHz clock is detected, it synchronizes its clock with the Master clock source and performs as a translator function for possible other KxLCN-type nodes on the network.

Figure 5 - Mixed Clock System (KxLCN Node Addition)

Translator failure

If there are multiple KxLCN nodes on a system,

- The failure of a translator node requires the establishment of a new translator.
- Upon the loss of the digital clock frame, all the KxLCN listener nodes switch to the subchannel mode to listen for the 12.5 kbaud clock message.
- All KxLCN nodes establish themselves as translators, and all of them send out clock synch messages at 5 Mbaud. This causes no harm.
- Each translator monitors LCN traffic for duplicate clock message frames.
- As the condition is detected by the multiple translator nodes, the translator node with the lowest LCN node address is allowed to remain as translator.
- The remaining translators simply stop sending the clock synch message frames and become listeners once again.

Clock signal—remote segments

The two NCF-defined, non-KxLCN clock source nodes must be located on the main LCN segment. If one or more remote segment contains all KxLCN nodes, the main segment must contain at least two KxLCN nodes. One KxLCN serves as the translator, which receives the 12.5 kbaud clock message and generates the 5 Mbaud clock message. The second KxLCN serves as a backup to the translator and automatically takes over the translation function if the primary translator fails.

If the remote segments contain non-KxLCN nodes, the additional clock hardware (FOCTs, FOCRs, and associated cabling) is required to transmit the 12.5 kbaud clock signal to the non-KxLCN nodes on the remote segments.

Example

Figure 6 shows another possible mixed clock system.

Operation

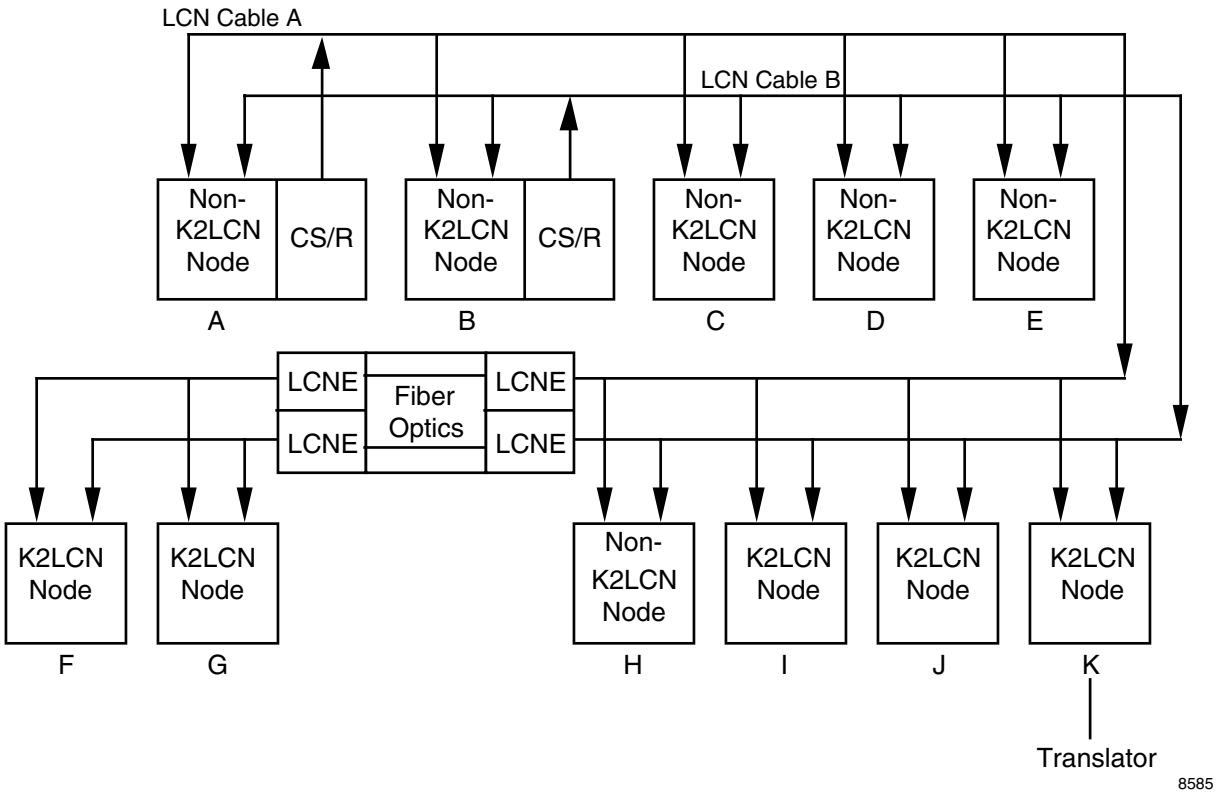
- The lowest numbered KxLCN node loaded assumes the role of translator (K).
- The remaining KxLCN nodes function as listeners in the digital mode.
- The translator node (K) listens for and uses the 12.5 kbaud clock for its own clock synchronization.
- The translator node (K) retransmits the clock message frame at 5 Mbaud on both cables.
- The 5 Mbaud digital clock message frame is used by the remaining KxLCN listener nodes, nodes F, G, I, and J.

NOTE: Without a KxLCN translator node on the main segment, KxLCN nodes F and G would never receive a clock message.

Translator Failure

On the main segment, if the translator node (K) were to fail

- Each of the KxLCN listeners (I and J) switch to the subchannel mode to listen for the 12.5 kbaud clock message.
- Both nodes I and J simultaneously establish themselves as translators.
- Duplicate clock messages are sent at 5 Mbaud.
- Eventually, the node with the higher LCN node address drops out and the node with the lowest address remains as the translator.



A = Assumed to be configured as a clock source and loaded first. Provides the clock data to the CS/R board for transmission at the 12.5-kHz frequency. The clock is superimposed on the 5-MHz LCN signal on its cable. Once Master is established, listens to nobody. Will assume responsibility of Slave clock source when recovering from a failure.

B = Assumed to be configured as a clock source and loaded after the other configured clock source. Once Slave is established, listens to clock generated by the Master clock source, synchronizes its own clock, and provides the clock data to be transmitted by the CS/R board on the other cable at the 12.5-kHz rate. Will continue to transmit the clock if the Master clock source fails. At this time it declares itself as Master.

C, D, E, H = Listens for the 12.5-kHz clock on cables A and B.

K = Assumed to be the first KxLCN-type node to be loaded after the clock source is powered up. First listens to both cables for a digital mode clock sync message frames. If none is detected, it switches to the Subchannel Mode and listens for the 12.5-kHz clock signal. If a 12.5-kHz clock is detected, it synchronizes its clock with the Master clock source and starts to act as a translator function for the other new type nodes on the network.

F, G, I, J = Assumed to be loaded after node K becomes established as a translator. Listens for digital mode clock message frames on both cables A and B. Synchronizes its own clock using the digital clock sync message from the translator mode.

Figure 6 - Mixed Clock System (Multiple KxLCN Node Additions)

Clock Displays

R320 and later

There are clock status displays available on systems operating on R320 or later software. These displays provide status of the clock subsystem and incorporate support for the KxLCN board:

CLOKMODE	Provides the mode of clock operation in all nodes.
CLOKSYNC	Provides clock sync status for all nodes.
CLOKTRAN	Provides translator status for all nodes.
CLOKCABL	Provides clock cable selection status at each node.

R430 and later

On R430 and later systems, the clock displays listed above have been removed and the following displays have been added:

CLOKSTAT	Incorporates all the information previously provided by the four separate clock displays.

PERFMENU

Figure 7 shows the PERFMENU display that provides targets to access the clock displays.

R400

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PERFMENU - MENU OF PERFORMANCE AND LOADING DISPLAYS  SELECT | SELECT      R400
                                                     FOR PAGE 1|FOR PAGE 2

DATACHNG  -CONVENIENT MECHANISM TO ALLOW DISPLAY AND CHANGE OF POINT.PARAM VALUES
NODEPERF  -DISPLAYS SUMMARY OF ANY NODE'S PRIMARY PSDP DATA INCLUDING IMPORTANT NODE SPECIFIC INFORMATION
QUIKTRND  -CONVENIENT MECHANISM FOR GETTING POINT.PARAM DATA TRENDS; INCLUDING PSDP DATA FROM OPERATOR KEYBRD
$LNMENU   -CONVENIENT MECHANISM ALLOWS DISPLAY/RESET OF LCN DIAGNOSTIC VALUES FROM DIAI MEDIA
CPUCHKR   -SHOWS ALL SYSTEM NODES' CPUFREE VALUE AND ALLOWS A QUICK CHECK VALUE TO BE USED FOR COMPARISON TEST
PARCHKR   -SHOWS ALL SYSTEM NODES' PARSEC VALUE AND ALLOWS A QUICK CHECK VALUE TO BE USED FOR COMPARISON TEST
HEAPCHKR  -SHOWS ALL SYSTEM NODES' HEAPFREE VALUE AND ALLOWS A QUICK CHECK VALUE TO BE USED FOR COMPARISON TEST
             THESE TWO DISPLAYS ALSO ALLOW ACCESS TO HEAPFRAG
HEAPMIN   -SHOWS ALL SYSTEM NODES' MINIMUM HEAP VALUE & ALLOWS A QUICK CHECK VALUE TO BE USED FOR COMPARISON TEST

CHKPTIME  -CONVENIENT MECHANISM TO DISPLAY AND CHANGE CHECKPOINT OFFSET AND PERIOD INFORMATION
CLOKMODE  -ACCESS TO NODE CLOCK STATUS INCLUDING CLOKSYNC, CLOKTRAN & CLOKCABL DISPLAYS FOR K2LCN BOARDS BEGINNING WITH R320
AMDETAIL  -GENERIC ACCESS TO MANY OF THE AM'S PSDP PARAMETERS FOR THE SNAPSHOT PERIOD, CURRENT, AND PREVIOUS HOUR
AMTREND   -GENERIC TREND OF 16 OF THE AM'S PRIMARY PSDP PARAMETERS FROM 1 MIN TO 96 HOURS - REAL TIME ONLY
NGDETAIL  -GENERIC ACCESS TO MANY OF THE NG'S PSDP PARAMETERS FOR LOAD AND PERFORMANCE DETERMINATIONS
NGTREND   -GENERIC TREND OF 16 OF THE NG'S PSDP PARAMETERS FOR LOAD AND PERFORMANCE DETERMINATION FROM 1MIN-96HRS, RT ONLY
HMDETAIL  -GENERIC ACCESS TO MANY OF THE HM'S PSDP PARAMETERS FOR LOAD AND PERFORMANCE DETERMINATIONS
HMTREND   -GENERIC TREND OF 16 OF THE HM'S PSDP PARAMETERS FOR LOAD AND PERFORMANCE DETERMINATION FROM 1MIN-96HR, RT ONLY
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9300

R500

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PERFMENU - MENU OF PERFORMANCE AND LOADING DISPLAYS  SELECT | SELECT      R500
                                                     FOR PAGE 1|FOR PAGE 2

DATACHNG  -DISPLAY AND CHANGE ANY POINT.PARAMETER DATA VALUE
NODEPERF  -DISPLAY MAJOR PSDP DATA FOR A LCN NODE
QUIKTRND  -TREND POINT.PARAMETER DATA WITH SPECIFIED RANGES AND DATA CHANGE CAPABILITY
$LNMENU   -LCN STATISTIC DISPLAYS TOP LEVEL MENU
CPUCHKR   -ALL LCN NODE CPUFREE VALUES WITH "CHECKER" HILIGHTING
PARCHKR   -ALL LCN NODE PARSEC VALUES WITH "CHECKER" HILIGHTING
HEAPCHKR  -ALL LCN NODE HEAPFREE VALUES WITH "CHECKER" HILIGHTING
HEAPMIN   -ALL LCN NODE HEAPMIN VALUES WITH "CHECKER" HILIGHTING
HEAPFRAG  -ALL LCN NODE HEAPFRAG VALUES WITH "CHECKER" HILIGHTING
CHKPTIME  -DISPLAY AND CHANGE THE HM CHECKPOINTING PERIOD AND OFFSET
AMDETAIL  -TABULAR DATA ON AM OPERATION AND CHARACTERISTICS
AMTREND   -TREND DATA ON AM OPERATION AND CHARACTERISTICS

CLOKSTAT  -LCN CLOCK SUBSYSTEM OPERATION SHOWING MODE, SYNCH, CABLE, AND TRANSLATE STATUS
NGDETAIL  -TABULAR DATA ON NG OPERATION AND CHARACTERISTICS
NGTREND   -TREND DATA ON NG OPERATION AND CHARACTERISTICS
HMDETAIL  -TABULAR DATA ON HM OPERATION AND CHARACTERISTICS
HMTREND   -TREND DATA ON HM OPERATION AND CHARACTERISTICS
HISGRPS   -DISPLAYS THE HISTORY GROUP POINT CONFIGURATION FOR ANY UNIT AND GROUP NUMBER
SLTCONFG  -DISPLAY HG SLOT CONFIGURATION AND COMPARE WITH HARDWARE
UCNCOMM   -DISPLAY UCN COMM RELATED DATA AND OPERATION STATISTICS
UCNEVENT  -DISPLAY UCN EVENT TYPE DATA AND OPERATION CHARACTERISTICS
NIMTREND  -TREND DATA ON NIM OPERATION AND CHARACTERISTICS
UCNVERSN  -DISPLAY ALL UCN NODE VERSION AND REVISION DATA
IOPMDATA  -DISPLAY PM PRIM/SEC VERSION AND REVISION DATA INCLUDING IOP LEVEL INFORMATION
```

34475

Figure 7 - PERFMENU Display

Clock Translation display

The CLOKTRAN display shows all nodes' translation states.

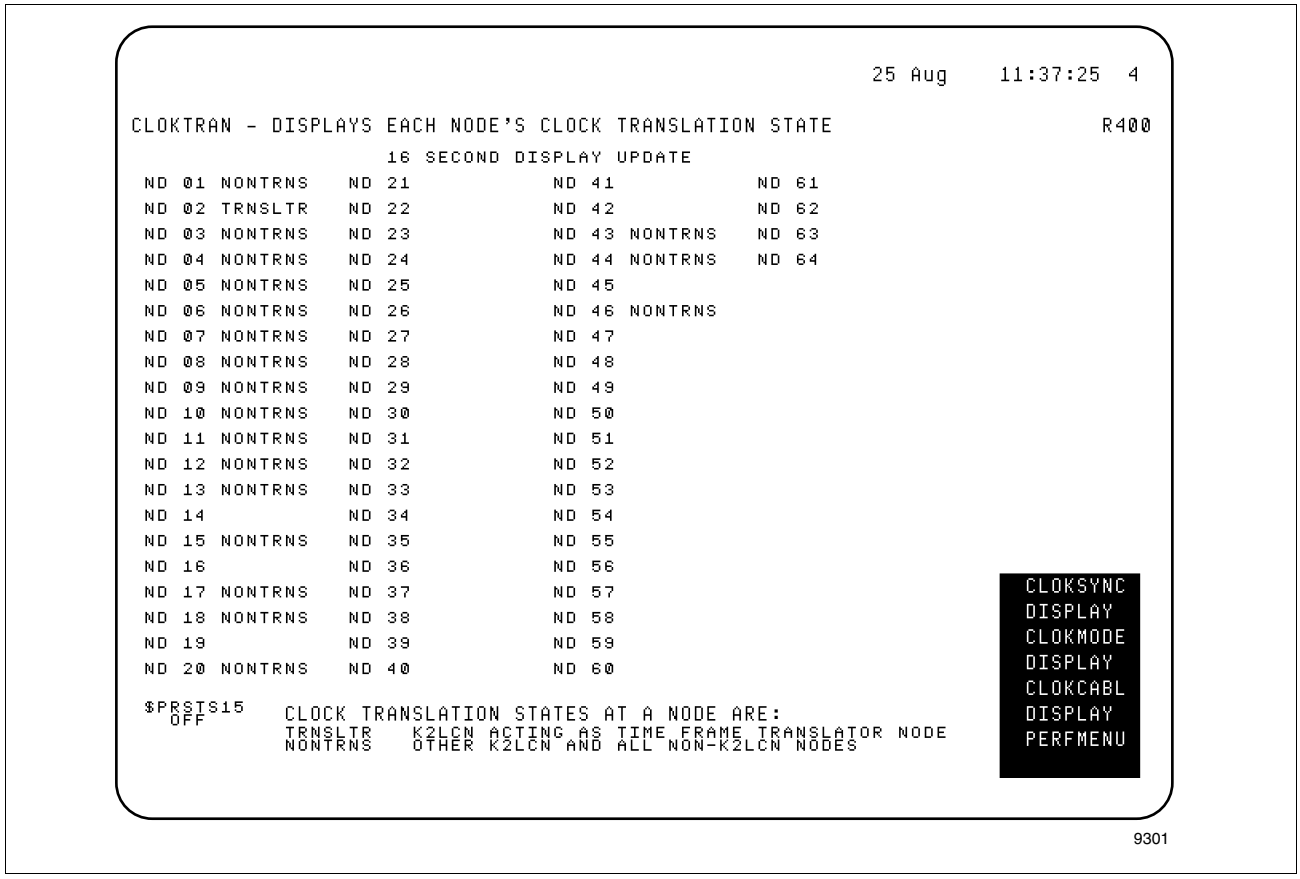


Figure 8 - Clock Translation Display (CLOKTRAN)

Clock sync display

The CLOKSYNC display provides a display of all nodes' clock synchronization statuses.

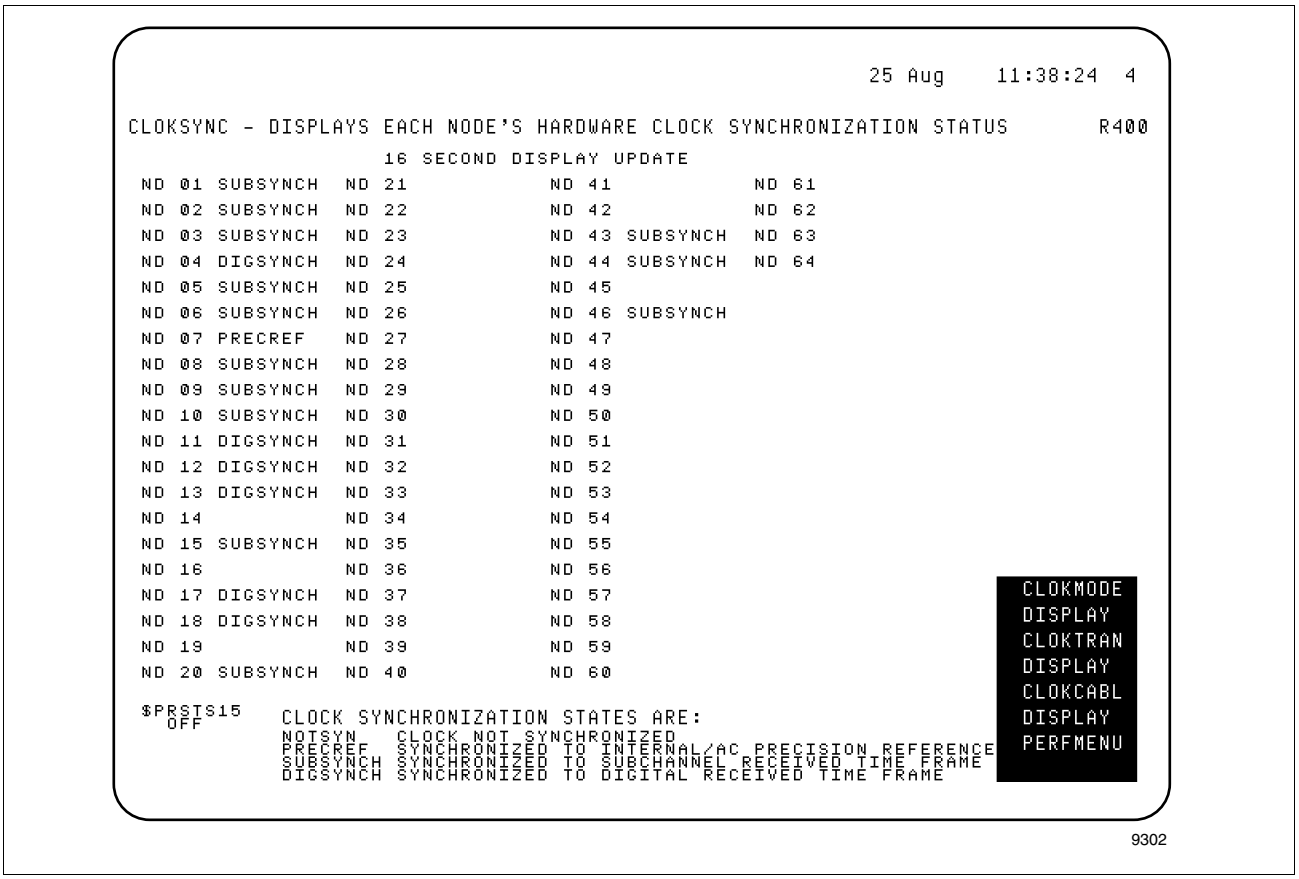


Figure 9 - Clock Synch Status Display (CLOKSYNC)

Clock operating mode display

The CLOKMODE display provides a display of all nodes' clock operating modes.

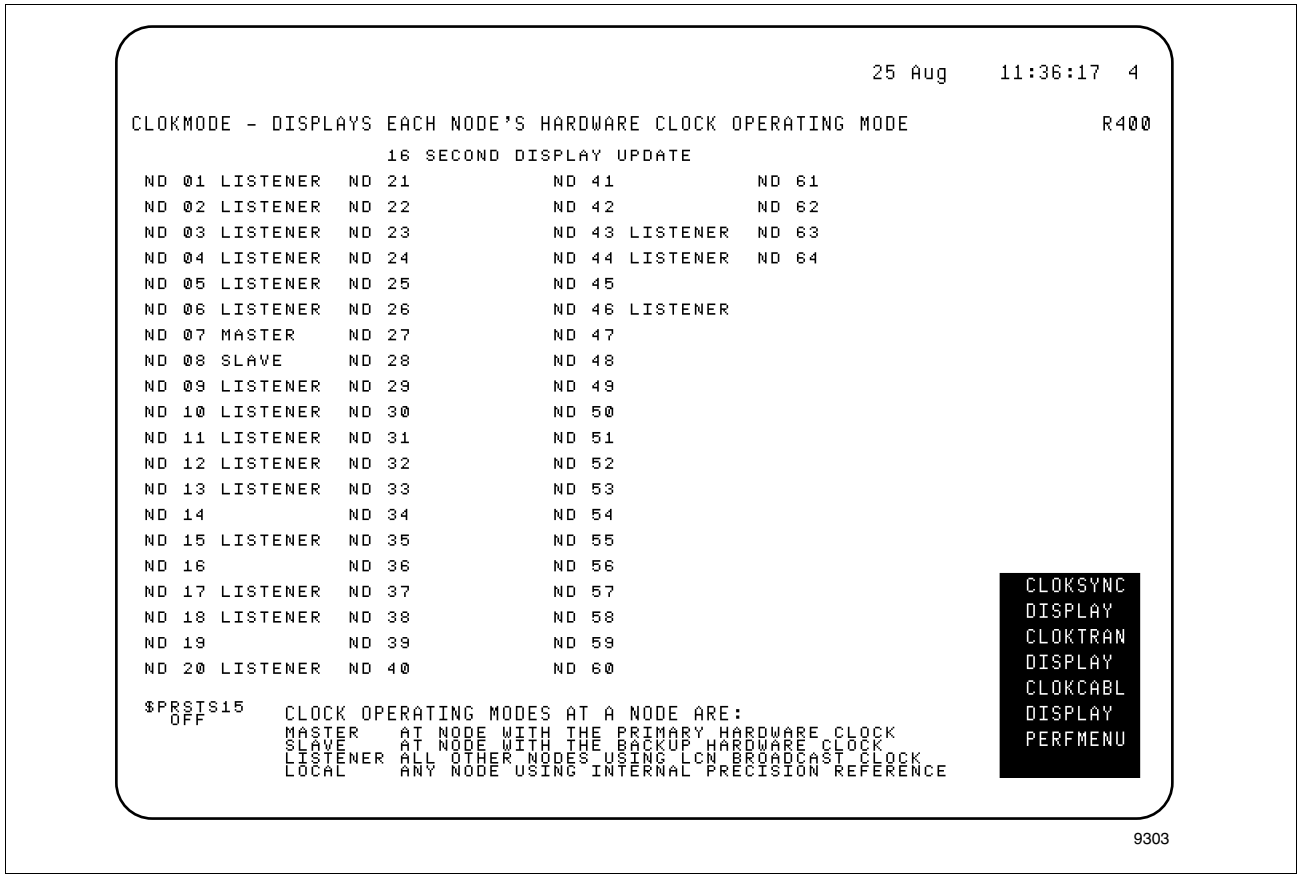


Figure 10 - Clock Operating Mode Display (CLOKMODE)

Clock cable selection display

The CLOKCABL display provides information on the cable in use for clock signals. The CLOKCABL display updates every 16 seconds.

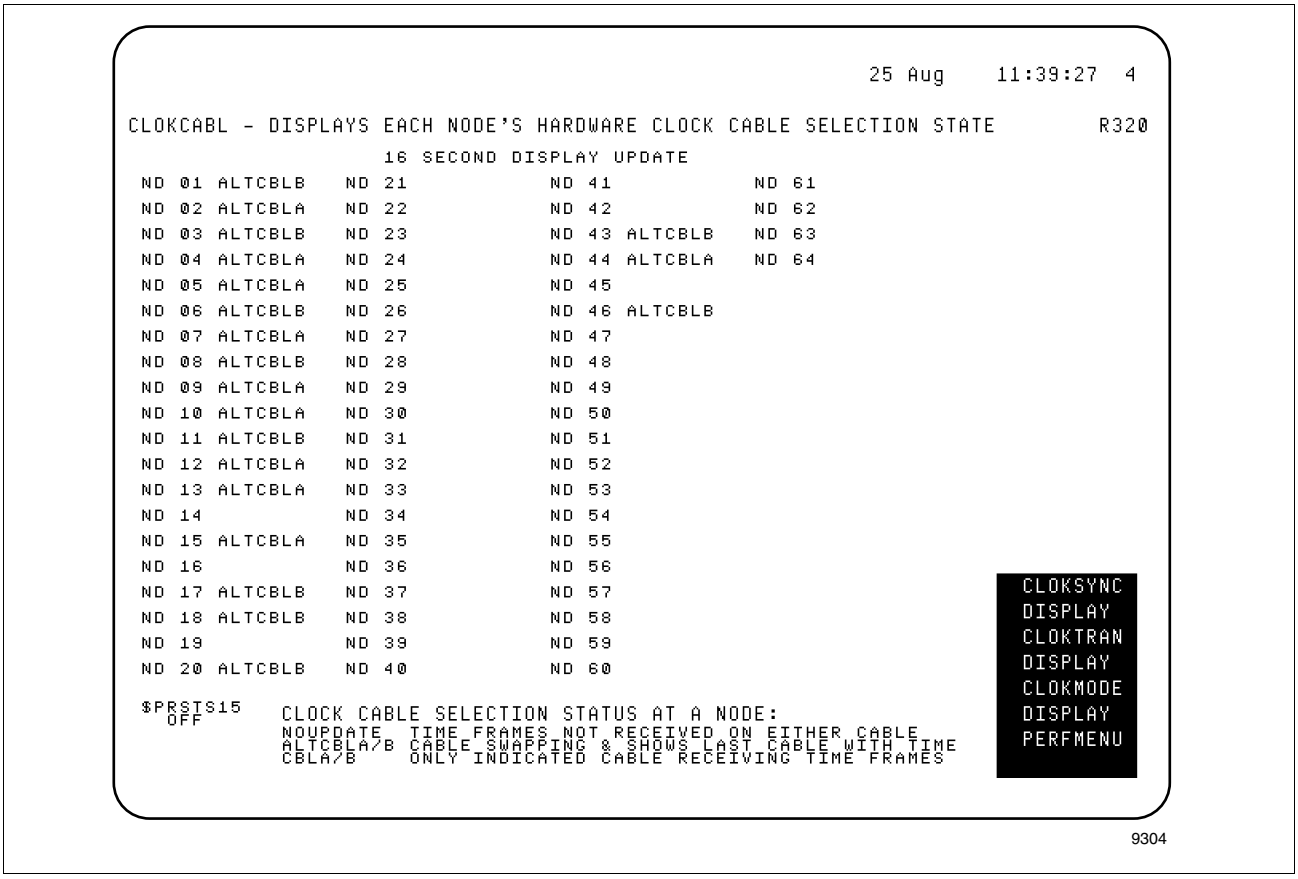


Figure 11 - Clock Cable Selection Display (CLOKCABL)

Clock Status display

The CLOKSTAT display (used on R430 and later) summarizes the information on the previous clock displays, providing the following for each node:

CLK_MOD	Clock operating mode
CLK_CBL	Information on the cable in use for clock signals
CLK_SYN	Clock synchronization status
CLK_TRN	Translation state

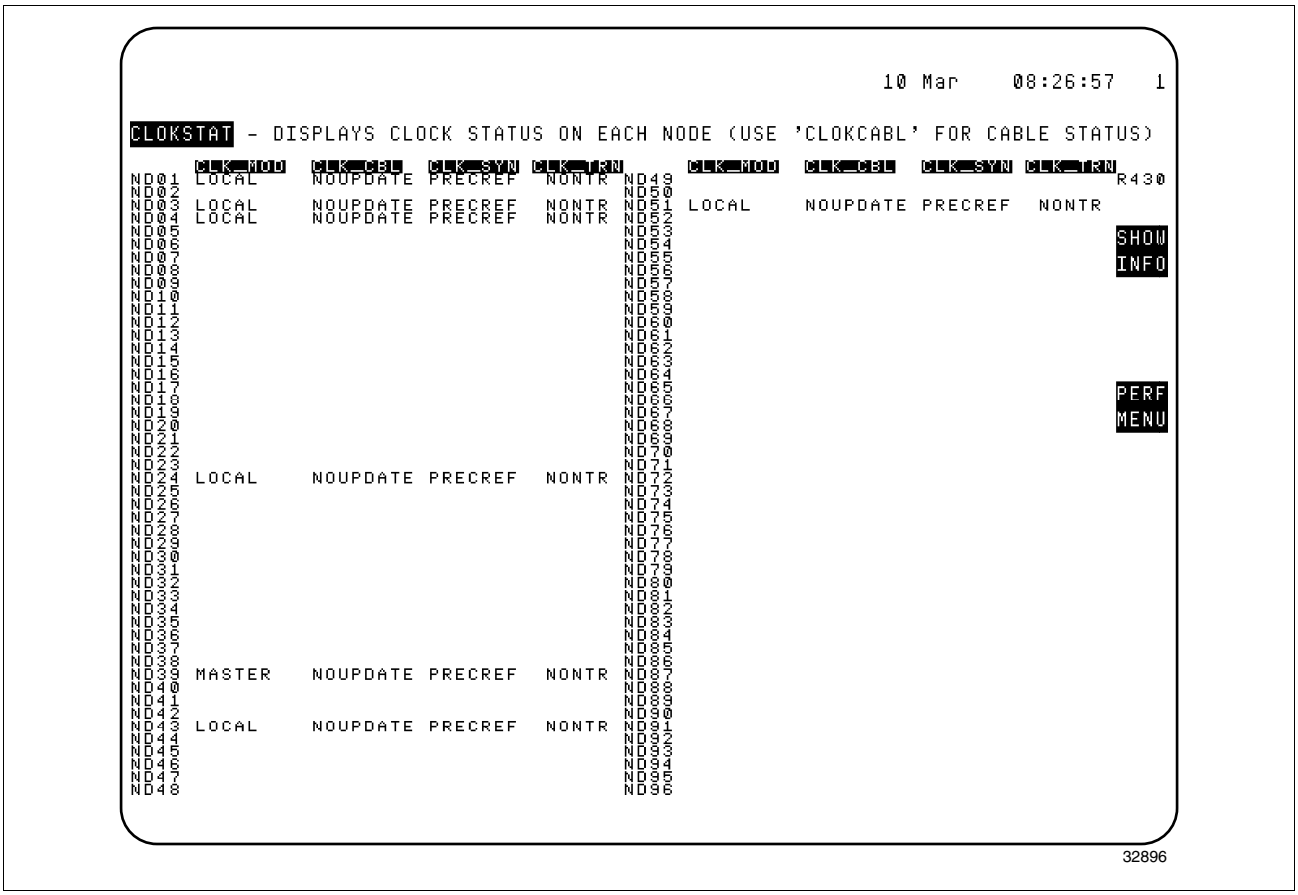


Figure 12 - Clock Status Display (CLOKSTAT)

Status indications

The following table describes the statuses indicated on the clock displays.

Table 2 – Clock Status Indications

Mode (CLOKMODE display or CLK_MOD status on CLOKSTAT)	
MASTER	Node is acting as clock master.
SLAVE	Node is acting as clock slave (backup master).
LISTENER	Node hears LCN clock signal/broadcast.
LOCAL	Node is using internal clock—cannot detect LCN clock.
Synch State (CLOKSYNC display or CLK_SYN status on CLOKSTAT)	
NOTSYN	Node is not synchronized with the LCN clock, to the ac power line, or to an external clock source.
PRECREF	A node (other than the clock master) is not synchronized to the LCN and is getting synch signal from either the ac power or an external clock source. Node is not synchronized with the LCN clock. Clock master always shows PRECREF, regardless if it is synchronized to the ac power line or an external clock source.
SUBSYNCH	Node is using "old" clock and is synchronized to the 12.5 kbaud signal. The lowest numbered KxLCN (the translator) indicates this status as well.
DIGSYNCH	Node is using "new" digital clock and is synchronized to the 5 Mbaud clock signal (any KxLCN that is not the translator).
Cable State (CLOKCABL display or CLK_CBL status on CLOKSTAT)	
CBLA CBLB	Node lost the time frame reference on one cable, and is now locked onto the opposite cable. CABLA-Node has a cable B clock problem and is using cable A. CABLB-Node has a cable A clock problem as is using cable B.
ALTCBLA ALTCBLB	Node sees normal clock operation—node is alternating between cables every 50 milliseconds. KxLCN nodes always shows alternating clock cable states.
NOUPDATE	The node is not "hearing" the LCN clock. The cable is using a local reference.
Translation State (CLOKTRAN display or CLK_TRN status on CLOKSTAT)	
TRNSLTR	Node is KxLCN acting as a translator in mixed clock systems. Normally, the lowest KxLCN node performs as translator, but certain conditions can leave another KxLCN correctly performing the translator functions.
NONTRNS	Node is nontranslating in the clock subsystem.

ATTENTION

ATTENTION—Clock Cable State
If a node is locked onto a particular LCN cable, periodically, the node attempts to alternate cables. If the display updates at the moment the node attempts to alternate, it indicates an alternating cable state (ALTCBLA/B).

ATTENTION

ATTENTION—Clock Translation State
Only the lowest numbered KxLCN node in a mixed system will translate.

Interpret “Suspect Clock” Messages

Description

To interpret “Investigate Suspect Clock” messages, go to the System Maintenance Journal.

Message format

In the System Maintenance journal, at the far right of the message, a field appears with the format:

`CLOKxx`

`xx` = a number from 00 to 08

Error codes

The following table describes the CLOKxx error codes.

Table 3 – CLOKxx Error Codes

Code	Description
00	Unknown cable communication error
01	Unknown cable data error
02	Unknown cable time update error
03	Cable A communication error
04	Cable A data error
05	Cable A time update error
06	Cable B communication error
07	Cable B data error
08	Cable B time update error

ATTENTION

ATTENTION—Use the Clock Status Word or LCN Cable Diagnostic displays to get additional troubleshooting information.

Clock Status Word

How to View the Clock Status Word Using SMCC

Purpose

The Clock Status Word indicates the alternating status of a non-KxLCN or translator node. It can also be used to determine if these nodes are having any problems receiving the clock signal on either cable. You can use SMCC (System Maintenance Control Center) to look at the Clock Status Word of any node on the LCN.

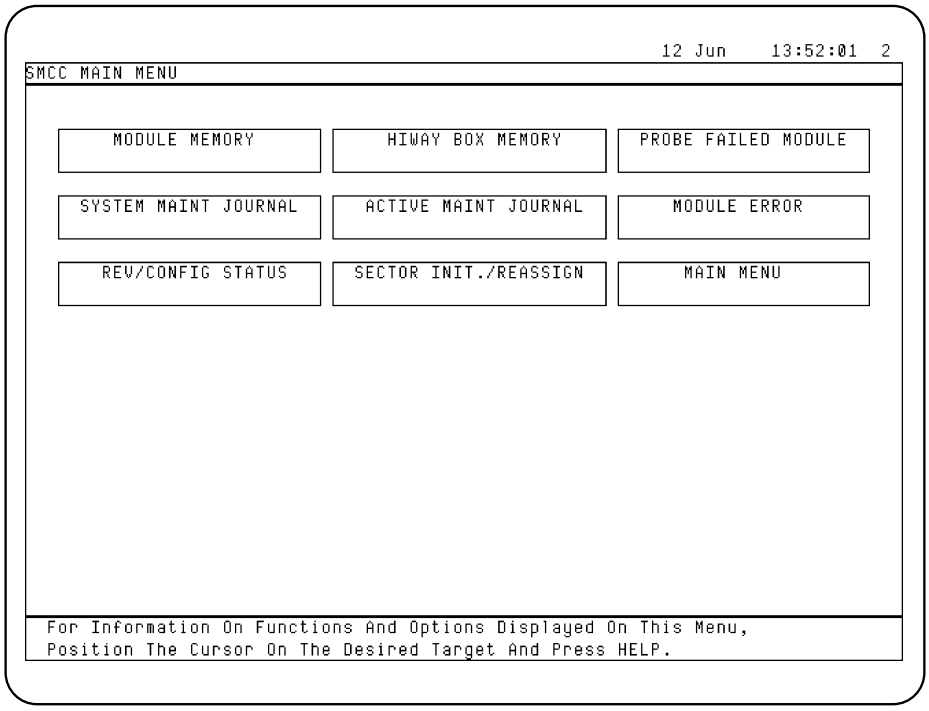
Requirements

The memory location of the Clock Status Word is different for different node types, processor types, personalities, and software releases. *On a given system/release, the location must be determined for each node/processor/personality type.* Determining the location requires going through two address pointers to locate the real memory location of the Clock Status Word; fortunately, the first pointer address is always the same for a given processor type.

Procedure

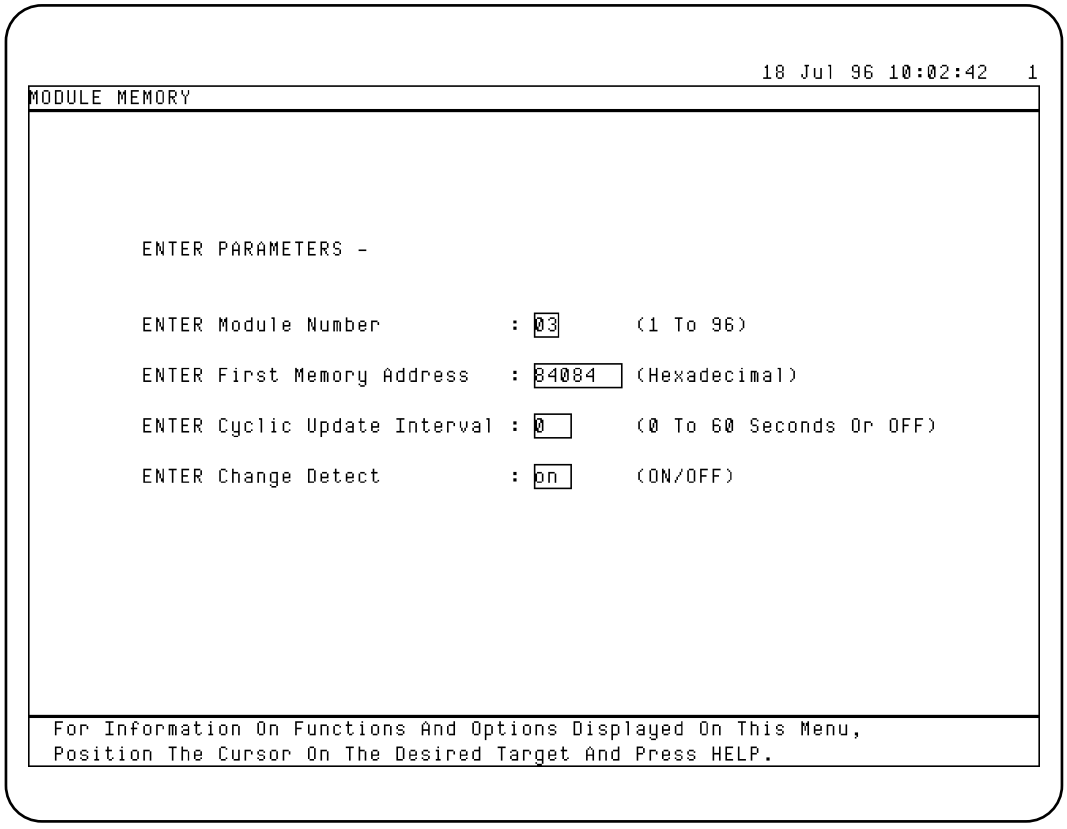
The following table describes the procedure to view the Clock Status Word.

Table 4 – Procedure to View the LCN Clock Status Word

Step	Action
1	At a Universal Station or GUS in the Engineering or Universal Personality, select SMCC/MAINTENANCE from the Engineering Main Menu. RESULT: SMCC Main Menu appears. 

Procedure, continued

Table 4 Procedure to View the LCN Clock Status Word, continued

Step	Action
2	Select MODULE MEMORY. RESULT: The Module Memory display appears.  34476
3	Type in the following parameters: a. Module Number—Enter LCN address of the node type you want to examine. b. First Memory Address— If the node processor is a 68000, enter **82084** (pre R500). If the node processor is a 68020, enter **84084**. NOTE: The values in this display are hexadecimal. c. Cyclic Update Interval— **0** (Updates the display at its fastest rate.) NOTE: The default entry is OFF. d. Change Detect— **ON** (Displays changed memory locations in white color.) NOTE: The default entry is OFF.

Procedure, continued

Table 4 Procedure to View the LCN Clock Status Word, continued

Step	Action
4	Press the [ENTER] key. RESULT: The memory location data appears. NOTES: 1. Each memory location is one 16-bit (2-byte) word. 2. The **first two words are the pointer** to the next memory location needed to determine the clock status word. This location varies depending on the software release, the processor type, node type, and the personality. EXAMPLE: In the example below, the first two words are 0009 88C6.

```
                                                    18 Jul 96 10:03:15   1
MODULE MEMORY DATA

          [ CHANGE DETECT RESET ]        [ PRINT DATA ]  [ $P1 ]

   64 CONSECUTIVE WORDS ARE DISPLAYED STARTING WITH FIRST ADDRESS

   o PRESS  MENU KEY TO RETURN TO MAIN MENU
   o PRESS  PAGE FWD/PAGE BACK KEY TO ADVANCE OR BACKUP DATA SETS
   o PRESS  ENTER KEY TO RE-DISPLAY SAME AREA (DEMAND UPDATE)

                        MODULE NUMBER 3

                 4 5   6 7   8 9   A B   C D   E F   0 1   2 3

   0084084      0009  88C6  0009  83E6  0009  829A  0006  0001
   0084094      0009  684A  0006  0001  0009  041A  0006  0001
   00840A4      0000  0036  0000  00B2  0000  0040  001A  0018
   00840B4      0008  42DA  0076  01BA  0009  8910  0009  8906
   00840C4      0009  8970  000A  250C  000A  0516  0009  8988
   00840D4      4E71  60FE  60FC  4E71  4E71  60FE  60FC  4E71
   00840E4      4E71  60FE  60FC  4E71  4E71  60FE  60FC  4E71
   00840F4      4E71  60FE  60FC  4E71  4E71  60FE  60FC  4E71

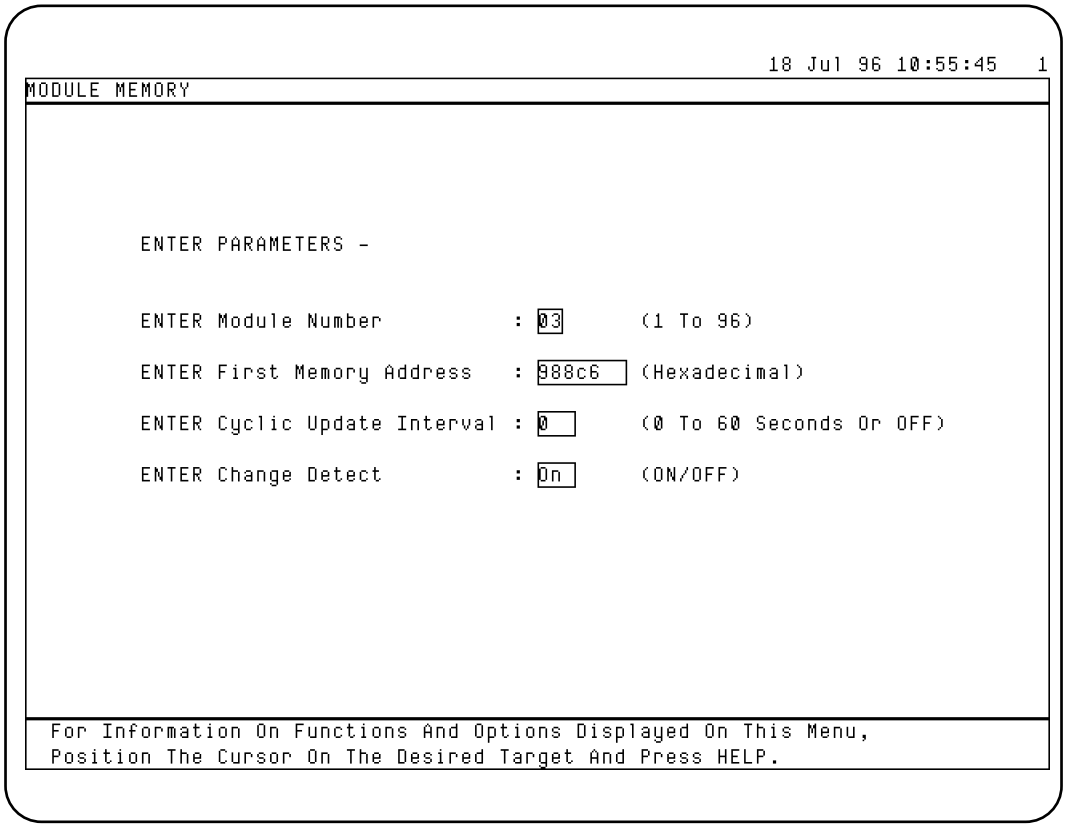
 For Information On Functions And Options Displayed On This Menu,
 Position The Cursor On The Desired Target And Press HELP.
```

34477

Procedure, continued

Table 4 Procedure to View the LCN Clock Status Word, continued

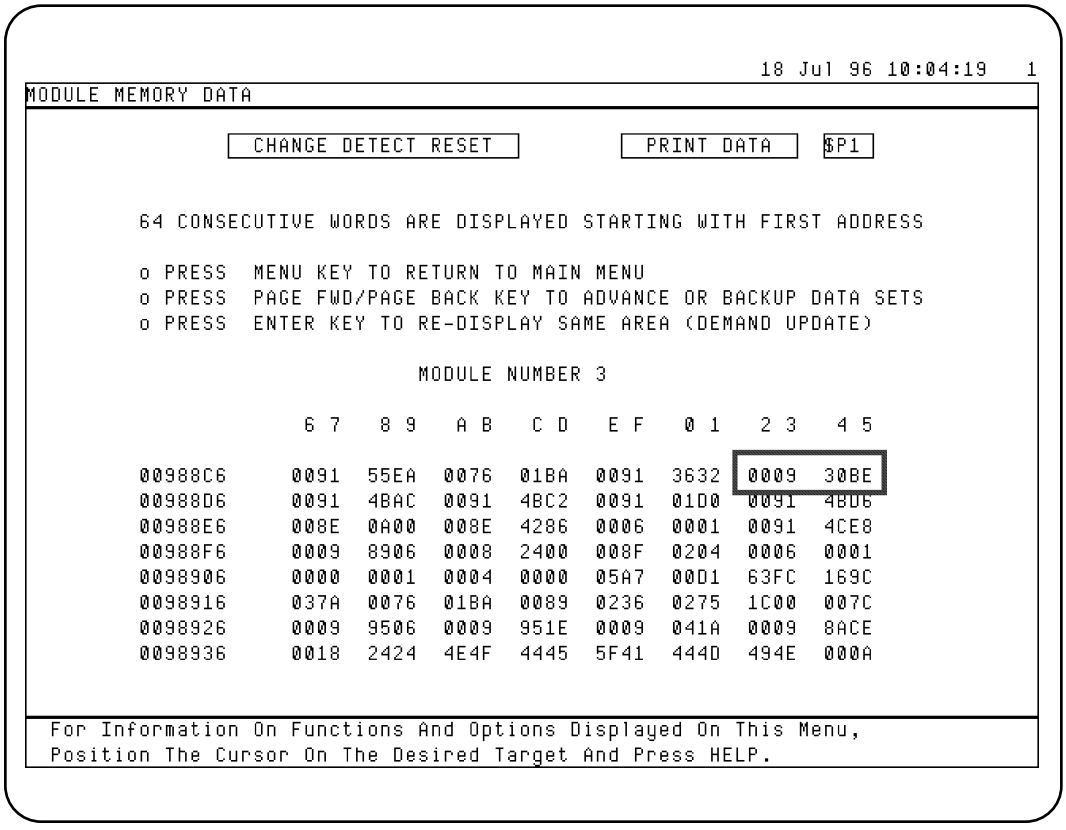
Step	Action
5	Press the [DISP BACK] key to return to the module memory display, then enter the address determined in the previous step and press [ENTER] EXAMPLE: In the example below, the address is 988C6.



Procedure, continued

Table 4 Procedure to View the LCN Clock Status Word, continued

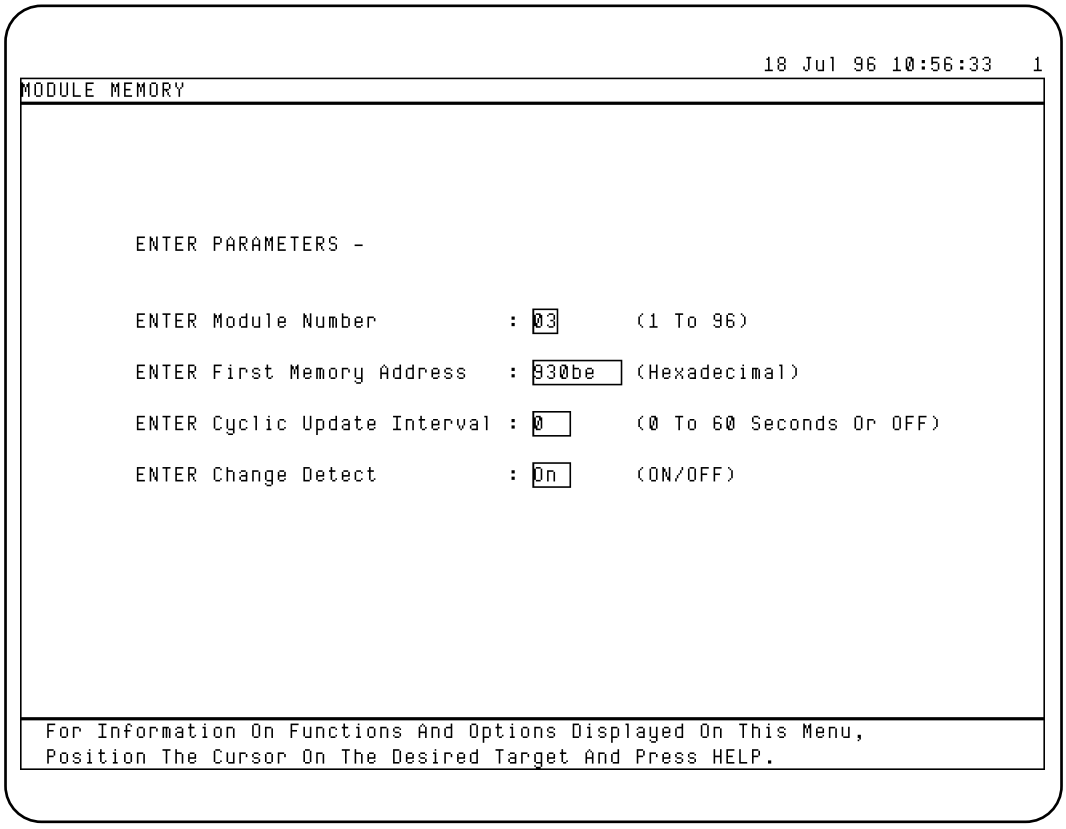
Step	Action
5 continued	RESULT: The memory location data appears. NOTE: The **last two words are the pointer** to the next memory location needed to determine the clock status word. EXAMPLE: In this example, the last two words now displayed are 0009 30BE.



Procedure, continued

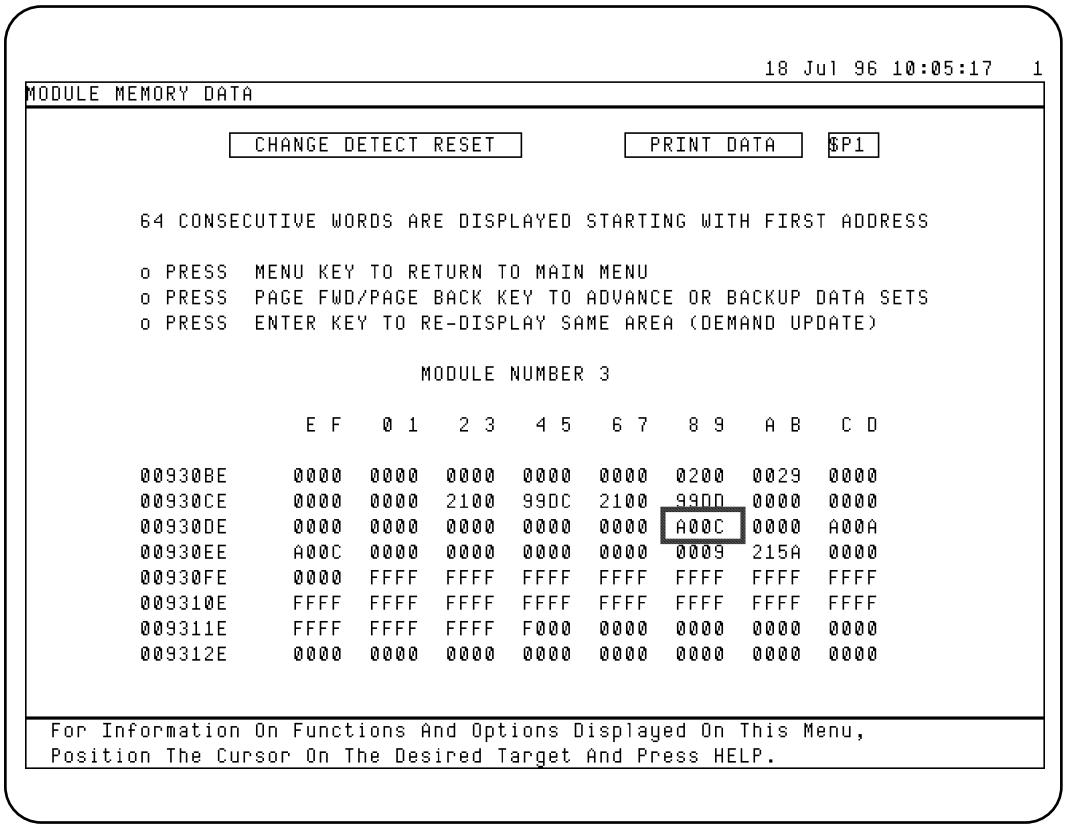
Table 4 Procedure to View the LCN Clock Status Word, continued

Step	Action
6	Press the [DISP BACK] key to return to the module memory display, then enter the address determined in the previous step. EXAMPLE: In the following example, the address 930BE was entered.



Procedure, continued

Table 4 Procedure to View the LCN Clock Status Word, continued

Step	Action
6 continued	RESULT: The memory location data appears. NOTES: 1. The Clock Status Word is located in the sixth word, three lines down. 2. You only need to do this once for nodes of a particular node type (such as a US), because **the Clock status Word location is the same for all node processor types on a particular software release with the same personality**. For the same node types, you can simply enter the final memory address, once it is determined. EXAMPLE: In the following example, the address 930BE was entered and the clock status word is A00C.  34483
7	Determine if Clock Status Word is “good” or “bad”, (see Table 5). Decode the clock status word, if necessary (see Table 6).

”Good” and “Bad” Clock Status Word Values

Description

Under normal operation, the clock subsystem alternates cables every 50 ms, resulting in the Clock Status Word in any non-KxLCN or translator node toggling between two correct “good” values (see Table 5).

If a node cannot hear the clock on a particular cable, its clock status word indicates a “bad” value (see Table 5).

Values

The following are “good” and “bad” clock status values in the hexadecimal format.

Table 5 – “Good” and “Bad” Clock Status Word Values

Node	GOOD Values		BAD Values	
	Value	Description	Value	Description
Listener Node (see Note)	A00A	Received cable A update	A002	Receiving only cable A updates
	A00C	Received cable B updates	A004	Receiving only cable B updates
Master Node	101A	Received cable A update	1012	Receiving only cable A updates
	101C	Received cable B updates	1014	Receiving only cable B updates
Slave Node	601A	Received cable A update	6012	Receiving only cable A updates
	601C	Received cable B updates	6014	Receiving only cable B updates
NOTE: A translator node behaves as a listener node.				

Decoding the Clock Status Word

Purpose

After viewing the Clock Status Word by using SMCC, decode the 16-bit word to determine the current clock status.

Procedure

The following table describes how to decode the Clock Status Word.

Table 6 – Decoding the Clock Status Word

Step	Action	
1	Convert the Clock Status Word from hex to binary (see Table 8). Example: A00C = 1010 0000 0000 1100	
2	Interpret bits 10 through 15 and bits 1 and 2:	
	Bits 15,14	Mode: 00 = Master clock source mode is selected 01 = Slave clock source mode is selected 10 = Listener-only source mode is selected 11 = Local clock source mode is selected
	Bits 13,12	Sync Source: 00 = Clock is not synchronized 01 = Clock is synchronized to the power line 10 = Clock is synchronized to the received message interrupt
	Bits 11,10	Received Message Error Status (during the past 50 ms period): 00 = No error 01 = Communication error 10 = Invalid data code 11 = Invalid time update
	Bits 02,01	Cable Select Status (during the last 50 ms): 00 = Received no time update 01 = Received cable A time update 10 = Received cable B time update
	Bit 00	Time set in progress
	Bit 03	Receive alternate cable status (1=yes)
	Bit 04	Transmit active (master or slave status)
	Bit 05,06	Cable error count (during current one second)
	Bit 07	Interrupt queued
3	Compare the statuses you found in the Clock Status Word to those you should see in a system that is operating normally (see Table 7).	

Binary format

The diagram below illustrates the binary format of the Clock Status Word.

ABCD = hex values, each value representing 4 bits of the 16-bit word
0 - 15 = bit positions

A				B				C				D			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Example

Shown below is an example of a Clock Status Word in binary format (A00C = hex values).

A				0				0				C			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0

"Good" values

If you are not familiar with hexadecimal (or have forgotten how to use hex), here is a handy reference for interpreting the "good" clock status word values. The key bits to consider are bits 01 and 02, and 10 through 15.

Table 7 shows the binary format of "good" clock status word values.

Table 7 – Binary Format — "Good" Clock Status Word Values

101A (Master Clock):

1				0				1				A			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	0	0	0	1	1	0	1	0

- Bits 14 and 15—this node is the Master clock source
- Bits 12 and 13—the clock is synchronized
- Bits 01 and 02—the master node received the cable A time update

101C (Master Clock):

1				0				1				C			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0

- Bits 14 and 15—this node is the Master clock source
- Bits 12 and 13—the clock is synchronized
- Bits 01 and 02—the master node received the cable B time update

601A (Slave Clock):

6				0				1				A			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	0	0	0	0	1	1	0	1	0

- Bits 14 and 15—this node is the Slave clock source
- Bits 12 and 13 —the clock is synchronized to the received message interrupt.
- Bits 01 and 02—the master node received the cable A time update.

601C (Slave Clock):

6				0				1				C			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0

- Bits 14 and 15—this node is the Slave clock source.
- Bits 12 and 13—the clock is synchronized. to the received message interrupt.
- Bits 01 and 02—the master node received the cable B time update.

A00A (other nodes):

A				0				0				A			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0

- Bits 14 and 15 —this node is another node in the listener mode
- Bits 12 and 13—the clock is synchronized to the received message interrupt.
- Bits 01 and 02—the node received the cable A time update.

A00C (other nodes):

A				0				0				C			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0

- Bits 14 and 15—this node is another node in the listener mode
- Bits 12 and 13—the clock is synchronized to the received message interrupt
- Bits 01 and 02—the node received the cable B time update

Hex to Binary Conversion Chart

Description

The following conversion chart and documentation template will assist you in debugging problems associated with Clock Status Words.

Conversion chart

The hexadecimal-to-binary-to-decimal conversion chart is presented here for your convenience.

Table 8 – Hex, Binary, Decimal Conversion Chart

Hexadecimal	Binary	Decimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
A	1010	10
B	1011	11
C	1100	12
D	1101	13
E	1110	14
F	1111	15

Documentation

The Clock Status Word has the following hexadecimal format: ABCD. Use the conversion table above and the description of the clock status word (what each bit means) to determine the status of your clock signals.

Node number:_________

Clock Status Word memory location:___________

"A"=				"B"=				"C"=				"D"=			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Node number:_________

Clock Status Word memory location:___________

"A"=				"B"=				"C"=				"D"=			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Node number:_________

Clock status word memory location:___________

"A"=				"B"=				"C"=				"D"=			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Node number:_________

Clock status word memory location:___________

"A"=				"B"=				"C"=				"D"=			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Node number:_________

Clock status word memory location:___________

"A"=				"B"=				"C"=				"D"=			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Locating Crossed LCN Cables

Comparison of Methods For Locating Crossed LCN Cables

Description

The clock subsystem can be used to help locate crossed LCN cables (or diagnose cable problems in general) in a mixed or non-KxLCN system by looking to see on which cable the clock can be heard and on which cable it cannot be heard. This can be accomplished by determining the clock alternating status of each non-KxLCN node.

The clock subsystem cannot be used to locate crossed cables in an all KxLCN system. In this case, crossed cables can only be detected through use of the crossed cable display ($LNACCT) which involves LCN communication mechanisms but not the clock subsystem.

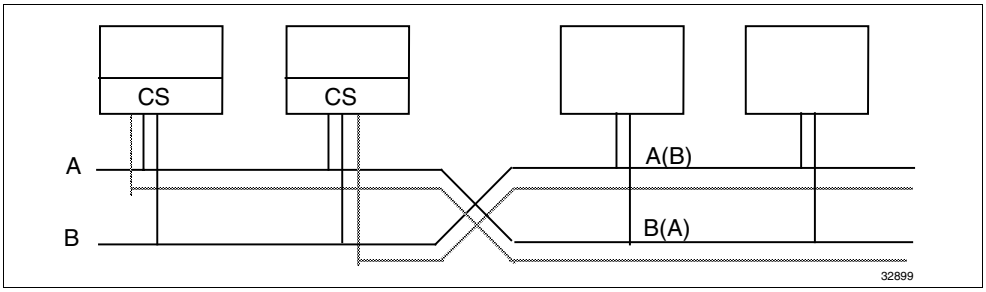


Figure 13 - Crossed LCN Cable Example

Methods

The are two methods for locating crossed LCN cables:

1. Determine the alternating status of non-KxLCN or translator nodes.

2. Use the Crossed Cables ($LNACCT) display.

The following table compares the methods for locating crossed LCN cables.

Table 9 – Methods for Locating Crossed Cables

Method		Advantage/Disadvantage
1	Determine the alternating status	Used to isolate the cross in non-KxLCN systems or can help narrow the location of the cross in mixed systems. Determine Clock Status Word in SMCC Provides an accurate representation of each non-KxLCN or translator node's alternating status (KxLCN nodes always show alternating), but is time consuming. Use CLOKCABL (R400) display or CLOKSTAT (R430 or later) display Not as accurate as the Clock Status Word, because of display update delays.
2	Use $LNACCT display	Provides the only solution for isolating crossed cables in an all-KxLCN system. Works for a mixed system as well. This method works on R430 and later if the lowest numbered US/GUS (the cable master) contains a K4LCN processor board or a K2LCN processor board with firmware revision P and hardware revision R or later.

Method 1—Procedure to Locate Crossed LCN Cables

Purpose

For an LCN segment where CS/R boards in clock master and slave nodes provide the clock signals, you can use the node's alternating status (determined by the clock status word or the CLOKCABL or CLOKSTAT display) to determine whether or not the segment has crossed LCN cables.

Indication

On systems using normally operating clocks, the CLOKCABL or CLOKSTAT display shows each node using either ALTCBLA or ALTCBLB. You should expect to observe the following:

- the clock alternates between the A and B cables every 50 milliseconds, and
- all nodes probably will not report using the same cable at the same instant.

After you know how to recognize the alternating status of nonKxLCN or translator nodes, it is a "process of elimination" to locate the node(s) with crossed cables. To determine if the cables are crossed, you must remove the clock signal from one of the cables.

Summary

By disconnecting one clock board at a time (in order to force non-KxLCN or translator nodes to a non-alternating clock status), it is possible to determine if the LCN cables are crossed at any non-KxLCN or translator node. This procedure works on any release of LCN software and any type of processor board, except KxLCNs.

Let us say you have crossed LCN cables and you decide to remove the clock source connected to cable B. The following is indicated because the cables are crossed:

- some of the nodes show clock updates on cable A
- other nodes show clock updates on cable B

Start at the end of your LCN and determine the alternating status for that node, then work your way toward the "middle" of the LCN in order to isolate the location of the cross.

ATTENTION

ATTENTION—Method 1 cannot find crossed LCN Extender fiber optic cables and is only for LCN segments using CS/R boards.

ATTENTION

ATTENTION—For non-translator KxLCN nodes:

- The Clock Status Word and the displays always show an alternating status (unless the node is a translator), regardless of whether or not the 12.5 kbaud clock message is present on both cables; consequently, they do not provide the user with helpful information.
- For all non-translator KxLCN nodes, the clock message is embedded in the 5 Mbaud signal.
- Translator nodes function like any non-KxLCN node, because they are receiving the 12.5 kbaud clock message.

WARNING

WARNING—If you find crossed LCN cables, you cannot safely reconnect the crossed cables while the system is controlling the process, because you will have to remove both the A and the B cables at the same time.

If the system is controlling the process, defer uncrossing the cables until the system can be taken off control; however, do not defer for a long time; operating with crossed LCN cables (coaxial or fiber optic) can cause a system failure if a cable malfunctions.

Procedure

The following table lists the steps to locate crossed LCN cables using method 1 to determine each node's alternating status.

Table 10 – Procedure to Locate Crossed LCN Cables—Method 1

Step	Action
1	Determine the Clock Status Word or call up the CLOKCABL or CLOKSTAT display. RESULT: All nodes should be alternating. Every active node displays either ALTCBLA or ALTCBLB. All nodes do not have to show the same cable, but all must indicate "ALT" (alternating). This means A and B cables are connected to each node and all nodes are receiving alternating clock messages. NOTE: You may still have crossed cables, but the electronics are OK. If this step fails, check for bad cables or faulty electronics.
2	Determine the two NCF defined clock source nodes: NOTE: Each clock source node must have a CS/R board; one node supplies the cable A clock and the other supplies the cable B clock.
3	Determine the clock master and slave nodes: • from the Clock Status Word, • from the CLOKCABL or CLOKSTAT displays, or • use the System Wide Values and Clock Source targets from the Engineering Main Menu.
4	Determine which nodes contain KxLCN processors, if any: • Use the CLOKTRAN or CLOKSTAT display to locate nodes marked TRNSLTR. • Use the CLOKSYNC or CLOKSTAT display to locate nodes marked DIGSYNCH. In steps 5 - 6, ignore the nodes marked DIGSYNCH.
5	Physically locate a master or slave node. Remove the coaxial T-connector from its CS/R board (leave the LCN cables connected). ATTENTION—To avoid unnecessary noise on LCN cables, do one of the following: • Ground the T-connector before removing it. or • Pull the T-connector halfway off to maintain its logic ground connection. RESULT: If there are no crossed cables, the Clock Status Words or the CLOKCABL or CLOKSTAT displays show either all CBLA or all CBLB at all active non-KxLCN or translator nodes on the system.

Procedure, continued

Table 10 Procedure to Locate Crossed LCN Cables—Method 1
continued

6	If the result of step 5 is not true, you probably have a crossed cable. Trace the cables and analyze the physical cable system. For example, if all but one node shows CBLA, the cables may be crossed between that node and the node that precedes it on the way from a CS/R board.
7	Uncross cables at the suspected node (remember the WARNING on page 49). RESULT: If the display shows either all CBLA or all CBLB at all active nodes, the problem is solved. Reconnect the T-connector you removed in step 5 and continue to step 8.
8	Reinstall the coaxial T-connector to the CS/R board.
9	Check the CLOKCABL display again after a few moments. Note: It might take up to five minutes for a system to show all nodes operating properly, although the reaction is usually much quicker. RESULT: ALTCBLA or ALTCBLB at all nodes is proper operation.

Limitations of Method 1 For Locating Crossed LCN Cables

Limitations of method 1

Method 1 (determining node's alternating status) has the following limitations:

- Cannot detect crossed LCNE fiber optic cables.
- Can be used only on LCN segments using CS/R boards.
- Is useful only for non-KxLCN and translator nodes.
- When the clock subsystem is damaged, the Clock Status Word or the CLOKCABL or CLOKSTAT display cannot dependably show which cable is receiving the clock signals.

Limitations of method 1

The following table describes the limitations of method 1 (Clock Status Word) and method 2 (CLOKCABL/CLOKSTAT displays) in locating crossed fiber optic cables.

Table 11 – Limitations When Locating Crossed Fiber Optic Cables

IF…	THEN…
LCNE fiber optic cables are crossed. FOCT/FOCR fiber optic cables are not crossed.	In a mixed or non-KxLCN system, the Clock Status Word and clock displays do not indicate crossed fiber optic cables, because the remote segment receives the clock signal through the FOCT/FOCR fiber optic cables, which are properly connected. See Example 1. in Figure 14.
FOCT/FOCR fiber optic cables are crossed. LCNE fiber optic cables are not crossed.	The Clock Status Word and clock displays indicate crossed cables, but the user should not conclude that the LCNE fiber optic cables or coax are crossed. See Example 2. in Figure 14.
NOTE: The Clock Status Word or the clock displays accurately detect crossed cables on a single segment.	

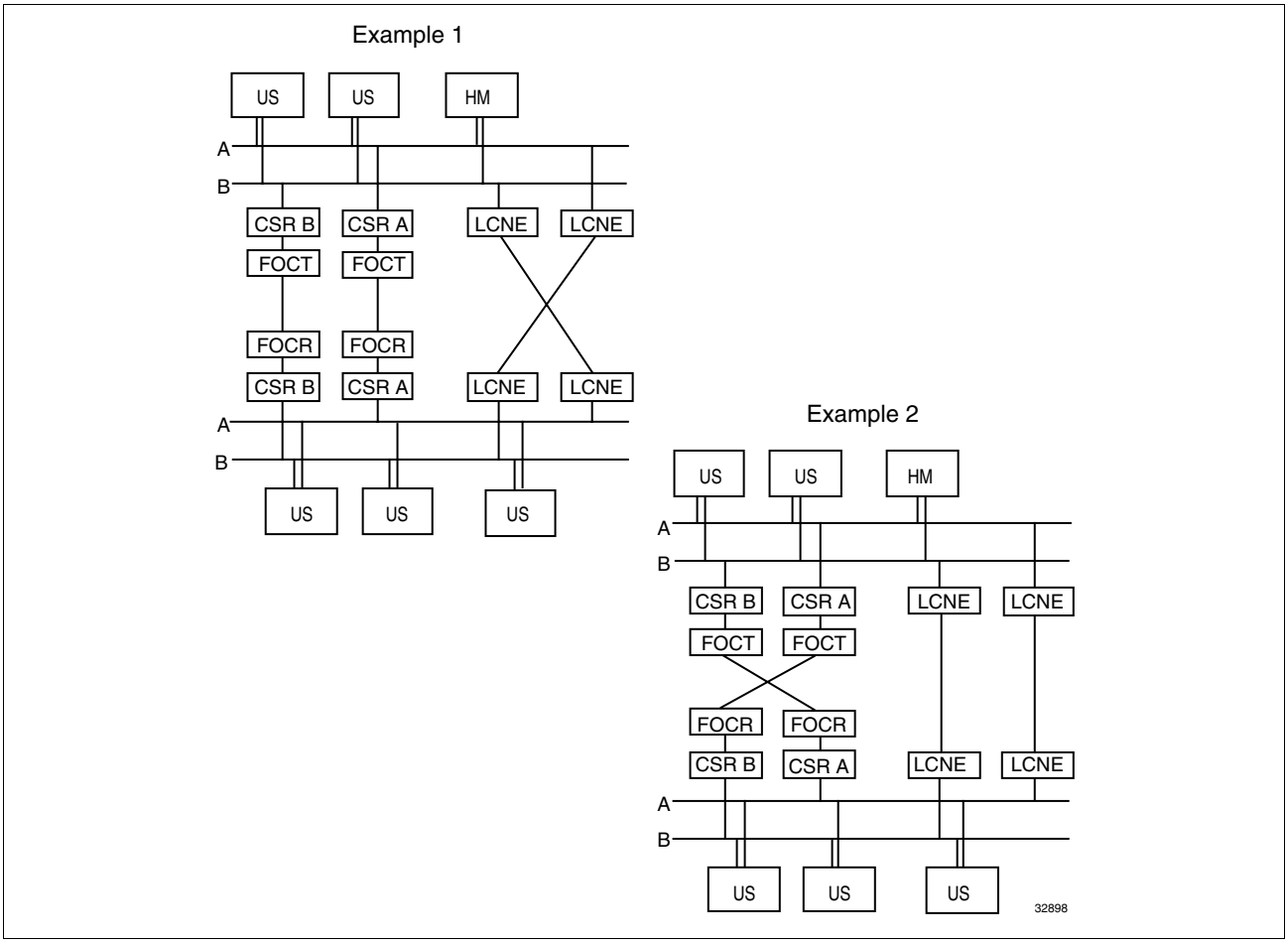
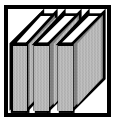


Figure 14 - Crossed LCN Cable Example



REFERENCE—The LCNI tests in HVTS can be used to check crossed cables not covered by method 1. For HVTS information, refer to *Hardware Verification Test System*, Binder TPS 3060-3

Method 2—Using Crossed Cable Display

Purpose

The Crossed Cable display ($LNACCT), available on R322 and R430 and later, provides the only solution for isolating crossed cables in an all-KxLCN system. It works for a mixed system as well. Here, we discuss a procedure you can use to check for crossed LCN cables by using the Crossed Cable display.

Requirements

This method of checking for crossed cables requires that the lowest numbered US/GUS (the cable master) have a K4LCN board or a K2LCN board with Rev. P or higher firmware and Rev. R or higher hardware.

Normal operation

The $LNACCT display shows a count received on each cable for each node. You should expect to observe the following:

- The cable master sends a count on only the active cable (differs from normal LCN communications, where messages are sent on both cables).
- Any node with crossed cables does not receive the count on the active cable port and, consequently, does not see the count. Most of the time, its counter on the $LNACCT display will be less than the rest of the nodes.
- The cable master always indicates one count higher than the other nodes.

ATTENTION

Occasionally, a crossed node picks up the count during the process of swapping LCN cables. For this reason, you should look at the display a few times over the course of 5 or 10 minutes.

Crossed cable display

The $LNACCT display (used on R322 and R430 and later) provides a count for each node that can be used to determine the location of crossed LCN cables. If the LCN cable master has a KxLCN board with Rev. P or higher firmware and Rev. R or higher hardware, it sends a count message on only the active cable. Any node with crossed cables will not see the message, so its count should be less than the others. Occasionally, a node with crossed cables will hear the count; this can occur if the master US/GUS has sent out the count before the crossed node has swapped cables. To obtain completely accurate information from this display, you should monitor it over a 5-minute period.

The cable master always indicates one count higher than other nodes.

In the example below, the lowest numbered US/GUS node (the cable master) is node 40.

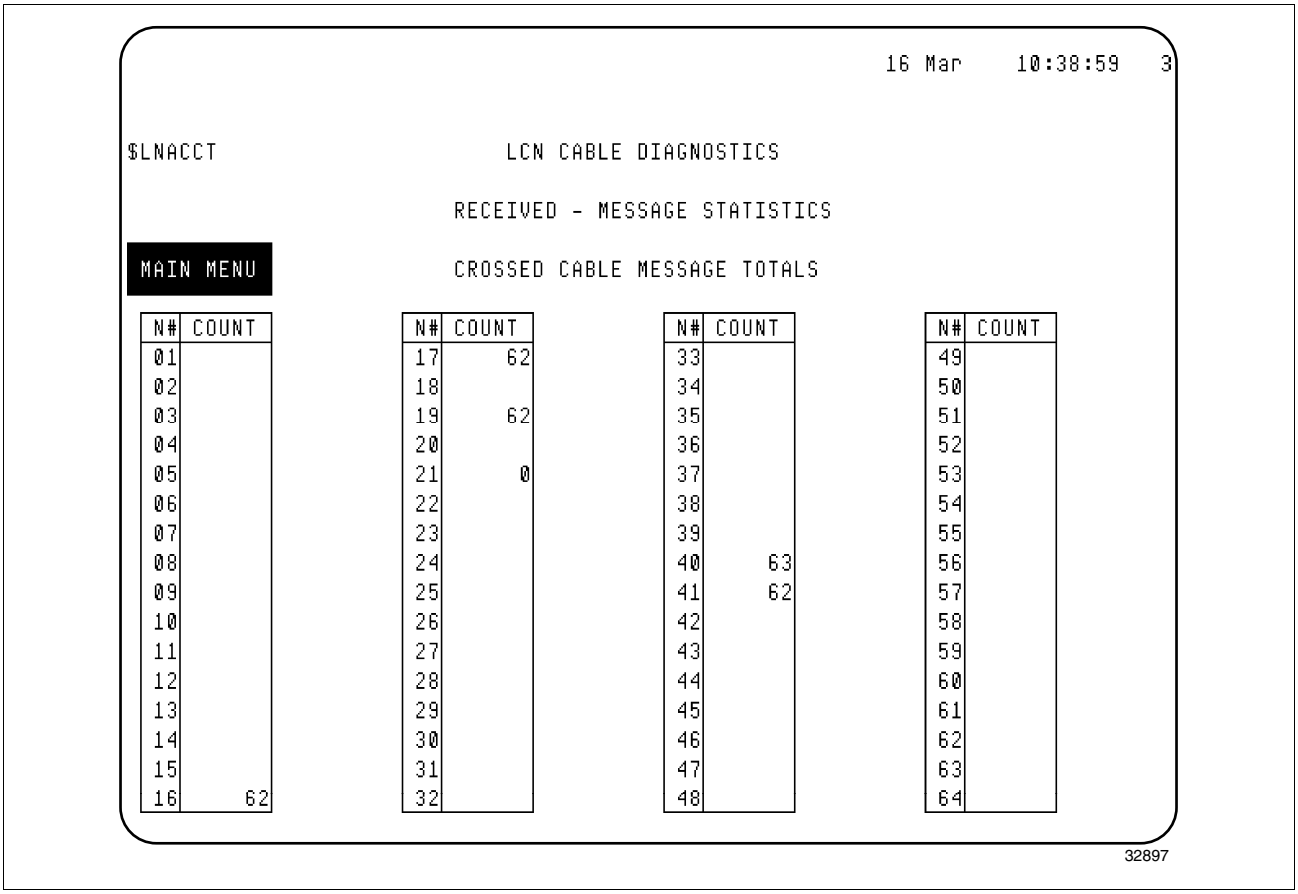


Figure 15 - Crossed Cable Display ($LNACCT)

Lab Exercise

Use Clock Displays

Introduction

The following exercise will familiarize you with the PERFMENU clock displays.

Duration

≈5 Minutes

Instructions

1. At your Universal Station, select the CLOKSTAT display from PERFMENU.

2. Identify the clock master, slave, and translator.

3. Are all nodes showing an alternating status?

4. Are all nodes synchronized to the network time?

Monitor Clock Status Word (Optional)

Introduction

The following lab exercise will help you become familiar with system clock functions by calling up the Clock Status Word for a node and monitoring it.

This lab exercise may require additional guidelines that your course manager will provide.

Duration

≈15 Minutes

Instructions

1. At your Universal Station, select the SMCC/MAINTENANCE target from the Engineering Main Menu .

2. Select MODULE MEMORY . Refer to the course material on how to read the Clock Status Word.

3. Determine the Clock Status Word for the master clock source, the slave clock source, and a non-KxLCN listner node or the translator.

4. Are all the nodes indicating an alternating status?

End of Lab Exercise

Find Crossed Cables

Introduction

The following optional lab exercise allows you to practice using the system clock to troubleshoot a crossed-cable connection.

Your course manager will set up the system before lab by crossing cables at an LCN node. Your course manager may provide additional guidelines required for the system on which you will perform the exercise.

You will need to have a topology map to complete this lab.

Duration

≈15 Minutes

ATTENTION

This lab can be performed only on an LCN system that is separate from the Training Lab or process-connected system. This lab may cause LCN nodes to go isolated.

Instructions

1. Determine the master clock source and slave source from the clock status word, from the NCF, the CLOKMODE, or from the CLOKSTAT display.

2. Disconnect the LCN cable from either the master or slave clock source.

3 Locate the crossed cables by determining each node's alternating status, either by calculating the Clock Status Word or from the CLOKSTAT display.

4. After you have located the cross and have discussed it with your course manager, call up the $LNACCT display to verify your determination.

5. Reconnect the cables to the correct LCN.

End of Lab Exercise

LAST PAGE