DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

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TITLE Field Installation/Acceptance

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ECO CHANGE	00003	A SHIMER	9-12-75	A Shimer	9/22/75

ENG	APPD	SIZE	CODE	NUMBER	REV
A Shimer	G. Wellbrock	A	SP	LPS11-E-5	A

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE Field Installation/Acceptance

1.0 SCOPE

Section 2. Introduction
Section 3. LPS11-E Field Installation
Section 4. LPSAM-E Field Checkout/Acceptance
Section 5. LPSDA Field Checkout/Acceptance

The LPS11-E may contain any configuration of from Ø to 6 LPSAM-E's and from Ø to 4 LPSDA's. This document can be used for Field Installation/Acceptance of any combination of these options by simply using the sections that pertain and ignoring the sections that deal with options not installed in the particular configuration.

2.0 INTRODUCTION

2.1 LPS11-E OVERVIEW

The LPS11-E is basically a backplane into which LPSDA and LPSAM-E options may be plugged. It also contains an M784 Bus Receiver for digital signals from the LPS, M957 Connector Module for LPSDA output connections, and (3) three cables for connecting the LPS11-E to an LPS11. All power and signals are derived from the basic LPS via these cables. A basic LPS11-S therefore, is a prerequisite for an LPS11-E.

2.2 LPSAM-E OVERVIEW

The LPSAM-E is a (4) four module option. It provides for (8) eight analog input connections and circuitry for selecting one of those (8) eight inputs and routing the selected signal to the output of the LPS11-E. This output is in turn routed to the basic

SIZE	CODE	NUMBER	REV
A	SP	LPS11-E-5	A

LPS where the signal is converted by the LPSAD-12.

It may be seen, therefore, that an LPSAD-12 and LPS11-E are a prerequisite for an LPSAM-E.

The (4) four modules that make up an LPSAM-E follow:

(1) M957 Connector module
(2) G728 Jumper modules
(1) A407 8 channel multiplexer

One further explanation is necessary. Up to (2) two LPSAG's or LPSAG-VG's Preamplifier options may replace either or both of the G728 jumper modules in an LPSAM-E. In this case, an A242 or A241 module will ship installed in the unit and the G728 jumper modules which are removed will ship as loose pieces.

2.3 LPSDA OVERVIEW

The LPSDA is a (1) one module option. It converts digital signals, from the LPSVC option in the basic LPS, into analog and routes the analog to the output connector provided in the LPS11-E. Each LPSDA has 2 channels. The prerequisites for an LPSDA are an LPS11-E and LPSVC.

The (1) one module that makes up an LPSDA is:

(1) A625 Dual D-A converter.

3.0 LPS11-E FIELD INSTALLATION

3.1 CABINET MOUNTING

Since analog cable lengths must be kept to a minimum, two

restrictions are made on system configurations:

1) The basic LPS11 must be rack mounted.

2) The LPS11-E must be mounted in the same rack immediately above or below the basic LPS.

3.2 BASIC LPS PREPARATION

NOTE: If the LPS11-E is not an add on to an existing LPS, then skip to section 3.4.

3.2.1 For access, remove top and left side covers to the basic LPS.

3.2.2 If an LPSVC (M7019 module) is present, then ECO #M7019-00002 (Scope Control Module) is required to invert the LDØØ-Ø7 lines to low going signals for bussing to the LPS11-E.

Identify this ECO by checking that E1 on the M7019 is a 7417 IC and not a 7416.

3.2.3 If an LPSAD-12 is present, then ECO #M7018-00003 (A/D Control Module) is required to provide for an increased settling interval.

Identify by checking that C43 is 4700 pf and C53 is 3300 pf on the M7018.

3.2.4 If one or more LPSAM-E's are included in the particular configuration being installed, then the settling interval must be increased to 15 μsec. by moving two jumpers on the M7018.

a) The PST Delay (E39) jumper must be moved from the split lug associated with C52 to the split lug associated with C43.

b) The MC Delay (E33) jumper must be moved from the split lug associated with C44 to the split lug associated with C53.

3.2.5 Install LPS11-E Power Harness #2, PN 7009789 in the basic LPS11 as follows:

STEP 1: Remove the LPS Power Supply for access to backplane. (4 screws, bottom of chassis)

STEP 2: Pull off the following power wires from backplane (solderless connectors). (Refer to drawings D-AD-7009110 AND D-UA-LPS11-S-Ø IN THE LPS print set for a rear view of the backplane):

1) WHT wire from FT 7-1.
2) ORN wire from FT 8-1.
3) BLU wire from FT 9-1.

STEP 3: Connect harness (7009789) and reconnect LPS wires as follows. (Care must be taken not to pinch machine wrapped wires):

1) BLK wire (Qty. 1) to FT 15-1.
2) RED wire (Qty. 1) to FT 11-1.
3) BLU wires (Qty 2) to FT 9-1 (Piggy Back).
4) ORN wires (Qty 2) to FT 8-1 (Piggy Back).
5) WHT wires (Qty 2) to FT 7-1 (Piggy Back).

STEP 4: Install mate n' locks in precut holes at right rear of LPS with J2 at right (nearest corner) and J1 to left as viewed from front of LPS.

STEP 5: Dress wires near backplane and rear panel and replace the LPS Power Supply (4 screws).

3.2.6 Connect LPS11-E Logic Cable (7009790) to basic LPS as follows:

STEP 1: Remove all modules above row 6 for access to M996 berg connector board.

STEP 2: Remove rear mounting panel (REF D-UA-LPS11-S-Ø ITEM 16 IN THE LPS PRINT SET)(PANEL UNDER UNIBUSS SLOT) (5 SCREWS)

STEP 3: Route the end of logic cable marked J1 (CAUTION: CABLE IS NOT A 1 TO 1 CONNECTION) THROUGH rear access underneath unibus, between rear module guides for rows 5 and 6 and connect to Expansion Berg (third connector from rear) on M996, A to A and VV to VV. Dress shielded TWP cable against PC board between berg connectors.

STEP 4: Replace modules (refer to D-MU-LPS11-S-1 Module Utilization). If Digital I/O Option is present, care must be taken not to dislodge any of the berg connectors

when replacing the module in row 5. One of the Mylar Electro-magnetic shields may be used as a shoehorn.

STEP 5: Replace rear mounting panel (5 screws).

3.3 LPS11-E Hook-up

3.3.1 Install LPS11-E Power Harness #1 (7009788).
Step 1: Plug G772 power connector module located at one end of the cable into slot A26.
Step 2: Plug mate n' locks (at the opposite end) P2 to J2 (located at left rear of basic LPS as viewed from the back - it is the jack nearest the corner) and P1 to J1.

NOTE: Since plugs are identical care must be taken not to swap them as they are power connections.

3.3.2 Connect the 'J2' end of the logic cable (7009790) TO THE I/O Adaptor module 5409209 (A to A and VV to VV) and plug module into B19.

3.4 POWER CHECK

Power up basic LPS and take the following voltage checks in the LPS11-E.

SCOPE POINT	VOLTAGE
B1D2	+15 VDC
B1E2	-15 VDC
B2A2	+ 5 VDC

4.0 LPSAM-E FIELD CHECKOUT/ACCEPTANCE

4.1 Equipment and documents required.

4.1.1 EDC VS-11 N or equivalent.

4.2.1 LPS Test 1, (MAINDEC-11-DAPSA, D & PB).

4.2 Determine whether or not the LPSAM-E channels to be tested have pre-amplifiers or not by examining the following module slots for A242 or A241 preamps and correlating with the key sheet.

SLOT	CHANNEL #'s
AB18	24 - 27
AB16	20 - 23
AB15	34 - 37
AB13	30 - 33
AB12	44 - 47
AB1Ø	40 - 43
ABØ9	54 - 57
ABØ7	50 - 53
ABØ6	64 - 67
ABØ4	60 - 63
ABØ3	74 - 77
ABØ1	70 - 73

1) For all channels without preamps, follow the procedure detailed in Section 4.3 of this document for a functional test of the LPSAM-E.

2) For all channels with preamps, follow the procedure detailed in Section 4.4 of this document for a functional test of the LPSAM-E.

4.3 FUNCTIONAL CHECK WITHOUT PREAMPS

4.3.1 Load LPS Test I and run 'C' Calibration routine, internal mode, as described in the diagnostic listing.

4.3.2 Set the EDC for 4.98047 volts with the polarity switch in + position, and connect '+' output to A17R1, '-' output to B10B1 and EDC ground to B10C2. To alleviate noise and offset due to ground loops, the EDC must be floated from

power line GROUND, . Set SR0-5 to 20_8, and perform the following steps in a loop until all existing channels have been checked.

STEP 1: CHECK for 7770 ±2 LSB in the LED display.

STEP 2: Set the EDC polarity switch to 'Ø' position. CHECK for 4ØØØ ±2 LSB in the LED display.

STEP 3: Set the EDC polarity switch to '-' position. CHECK for 0010 ±2 LSB in the LED display.

STEP 4: Change SR Ø-5 setting so as to add 1 to the present number (select next channel in sequence).

STEP 5: While observing the LED display, change the EDC polarity switch from '-' to 'Ø' to '+' position and leave it in '+' position.

CHECK that there was no significant change in the LED display while switching the EDC.*

STEP 6: Move the wire coming from the '+' EDC output to the next pin number in the chart below (apply voltage to next channel input in sequence).

CHECK to see if this new channel is present in the configuration. If not, all channels have been checked out (proceed to the next section). If the new channel is present in the configuration then GO TO STEP 1.

*Since the channel selected by SR Ø-5 at this point has a floating input the number in the LED display is indeterminable. But, whatever the reading may be, it should not change with the input voltage of another channel (i.e. from 0010 to 4000 to 7770).

	CH 20-27	CH 30-37	CH 40-47	CH 50-57	CH 60-67	CH 70-77
	LOC A17	LOC A14	LOC A11	LOC A8	LOC A5	LOC A2
X0	R1	R1	R1	R1	R1	R1
X1	L1	L1	L1	L1	L1	L1
X2	F1	F1	F1	F1	F1	F1
X3	B1	B1	B1	B1	B1	B1
X4	T2	T2	T2	T2	T2	T2
X5	N2	N2	N2	N2	N2	N2
X6	J2	J2	J2	J2	J2	J2
X7	D2	D2	D2	D2	D2	D2

CHART OF INPUT PINS

NOTE: The offset adjustment on the A4Ø7 multiplexer in LPSAM-E's is bypassed so that no gain or offset adjustment can be made in LPSAM-E's without preamps. Therefore, if the above checkout fails, a determination should be made as to whether all channels fail in the same manner or just a group of eight or just one.

1) If all channels are out slightly, the LPS Analog System Calibration Procedure (A-SP-LPS11-S-13) OR SECT 4.2 OF THE LPS MAINT. MANUAL SHOULD BE performed, and the above checkout repeated.

2) If all channels are completely out of the acceptable

range, then a more basic fault such as power or signal wiring should be investigated.

3) If a group of (8) eight or only (1) one channel fails, then the A407 Multiplexer is suspect.

4.4 FUNCTIONAL CHECK WITH PREAMPLIFIERS

This section pertains to LPSAM-E's that include A241 or A242 pre-amp options LPSAG or LPSAG-VG.

4.4.1 Connect EDC ground to pin B10C2 and make sure the EDC is floated from power line ground. Apply EDC voltages to the "+" and "-" inputs of each channel according to the tables below. Compare the readings in the voltage chart below. Converted values must be within ±2 LSB to be acceptable. As in Section 4.3 use the Calibration Routine of LPS Test I, and select the channel under test in SR Ø-5.

LED READINGS	EDC VOLTAGE
0000	-1V
1000	-0.750V
2000	-0.500V
3000	-0.250V
4000	0.000V
5000	+0.250V
6000	+0.500V
7000	+0.750V
7777	+1.000V

VOLTAGE CHART

CH	"+" Pin	"-" Pin
A	R1	T1
B	L1	N1
C	F1	J1
D	B1	D1
E	T2	V2
F	N2	R2
H	J2	L2
J	D2	F2

CH	SLOT	A17	A14	A11	A8	A5	A2
A		20	30	40	50	60	70
B		21	31	41	51	61	71
C		22	32	42	52	62	72
D		23	33	43	53	63	73
E		24	34	44	54	64	74
F		25	35	45	55	65	75
H		26	36	46	56	66	76
J		27	37	47	57	67	77

4.4.2 If checkout fails, it may be helpful in isolating the problem to replace the preamps with G728 jumpers and perform section 4.3 of this document.

5.0 LPSDA FIELD CHECKOUT/ACCEPTANCE

5.1 Equipment required

DVM capable of measuring 1 MV accuracy.

5.2 Calibration Check

5.2.1 LPSDA's are installed in LPS11-E slots as follows:

OPTION	CHANNELS	LOCATION
LPSDA #1	0 - 1	AB21
LPSDA #2	2 - 3	AB22
LPSDA #3	4 - 5	AB23

OPTION	CHANNELS	LOCATION
LPSDA #4	6 - 7	AB24

5.2.2 TOGGLE the following program into memory.

LOCATION	CONTENTS	COMMENT
30000	013737	Move
2	177570	SR Contents
4	170424	to EXT DAC REG
6	000774	Jump to Start

The number in the SR will be loaded into the EXT DAC register which has the following format.

15 - 13	12	11 — 0
CH #	UNUSED	DATA

*If the basic LPS has a starting address block other than 170400, this location must be changed accordingly.

5.2.3 Using the DVM and the above program, check the D-A outputs for as many channels as are configured. The SR settings, DVM readings and output pins are given below. Connect DVM ground lead to A21F2.

STEP NO.	CH. NO.	SR SETTING	OUTPUT PIN	DVM READING	ACTION IF OUT OF TOLERANCE
1		004000		0V ±1 MV	adj. top pot AB21
2	0	000000	A 20 R1	-5V ±1 MV	adj. 2nd pot AB21
3		007777		+4.997V ±2.5MV	go to step 1.
4		024000		0V ±1 MV	adj. 3rd pot AB21
5	1	020000	A 20 L1	-5V ±1 MV	adj. bottom pot AB21
6		027777		+4.997V ±2.5MV	go to step 4.
7		044000		0V ±1 MV	adj. top pot AB22
8	2	040000	A 20 F1	-5V ±1 MV	adj. 2nd pot AB22
9		047777		+4.997V ±2.5MV	go to step 7.
10		064000		0V ±1 MV	adj. 3rd pot AB22
11	3	060000	A 20 B1	-5V ±1MV	adj. bottom pot AB22
12		067777		+4.997V ±2.5MV	go to step 10.
13		104000		0V ±1 MV	adj. top pot AB23
14	4	100000	A 20 T2	-5V ±1 MV	adj. 2nd pot AB23
15		107777		+4.997V ±2.5MV	go to step 13.
16		124000		0V ±1 MV	adj. 3rd pot AB23
17	5	120000	A 20 N2	-5V ±1 MV	adj. bottom pot AB23
18		127777		+4.997V ±2.5MV	go to step 16.
19		144000		0V ±1 MV	adj. top pot AB24
20	6	140000	A 20 J2	-5V ±1 MV	adj. 2nd pot AB24
21		147777		+4.997V ±2.5MV	go to step 19.
22		164000		0V ±1 MV	adj. 3rd pot AB24
23	7	160000	A 20 D2	-5V ±1 MV	adj. bottom pot AB24
24		167777		+4.997V ±2.5MV	go to step 22.