Data
Systems

PHILIPS

Field Support Manual

UPL Master Slave Memory 1M8

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1.1 INTRODUCTION

The main memory module consists of a memory control card, one up to eight memory slave cards and a special backpanel for interconnection of these cards.
Each memory slave card contains 64K words of dynamic MOS Random Access Memory which features user transparent error correction. The memory is based on the MOSTEK MK4116-4 16K bit RAM chip which requires refreshing within every 2mSeconds. It is implemented in an array of 4 bars, each containing 21 chips, thus using a total of 84 devices for each 64K 21 bit word slave card. The 21 Bit word is allocated such that the 16 bits are for data and 5 bits for error correction. The total capacity for a complete memory module is 8 x 64K 21 bit words giving 512K words or 1M bytes.

The organization of the memory in 21 bit "words" has no effect on the byte organization of the host system. It is possible to read or write a 'word' or either left or right 'character', the timing and control for these various possibilities being provided by the memory itself.

Power failure detection and battery back-up facilities are optionally available at system level to save the memory contents in case of power failure. On the WMB 1 logic diagrams, all devices marked with a 'B' are supplied with battery back-up voltage. Read/Write memory cycles are forbidden during this time.

The refresh action is performed, as far as possible, "hidden" to avoid possible timing clashes with the master units on the System Bus, but it is ensured that all memory cells are refreshed within 2ms. Refresh is performed completely independent of the host system.

1.2 PHYSICAL DESCRIPTION

The Main Memory Module has been designed on cards of the double Euro-format and comprises of two different types of cards.

- The Memory Control Card WMC 1
- The Memory Slave Card WMB 1

Connection to the system bus is via the WMC 1 card only. The memory slave cards have no functional interface with the system, only power and OKI-OKO interfaces are present. Interconnection between the WMC 1 and the WMB 1 are via special backpanels depending on the memory capacity required.

For connector locations and pin allocations see the section INTERFACES. The physical positions of the memory control and the memory slave cards can be seen in Figure 1.10 upto 1.14.

1.3 TECHNICAL DATA

1.3.1 PERFORMANCE CHARACTERISTICS

OPERATING MODES

The memory has three basic operating modes:

- Read Cycle — Externally requested
- Write Cycle
- Refresh Cycle — Internally requested

DATA TRANSFER

The memory has the possibility to execute six types of data transfer:

- Read Word
- Read Left Character
- Read Right Character
- Write Word
- Write Left Character
- Write Right Character

STORAGE CAPACITY

- One Memory Slave Card has a useful capacity of 64K16 = 1048576 BITS
- Maximum Available Storage capacity 8 x 64K16 = 8388608 BITS
  OR 1MBytes
- Word Length 16 BITS
- Error Correction 5 BITS
- Total Word length (Data + Error Correction) 21 BITS

TIMING

- Typical Read Access Time = 570 nS. (445µs for High Speed Version)
- Typical Write Access Time = 195 nS. (173µs for High Speed Version)

ADDRESSING MODE

- Random Access

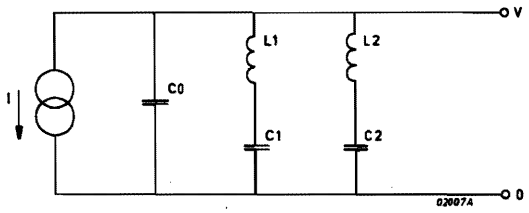
1.3.2 POWER REQUIREMENTS

Memory Control Card (WMC 1)

LOGIC NAME	NOM. VOLTAGE	tol%	MAX.AVERAGE CURR.			ΔI max (A)	f max (mc)	Co nF	C1 µF	L1 nH	C2 µF	C2 nH	max. rating (V)
			ope-rating	stand by	stand by batt.								
P5PU (+5VL)	5.05	4	2.3 (2.7)	2.3 (2.7)	0	0.2	1 (1.5)	1	1.5	0.	33	20	7
B5PU (+5VM)	5.05	4	1.2	1.2	1.2	0.1	1 (1.5)	-	1.0	0.	33	20	7

Note: Values in between brackets for "High Speed Version"

Table 1.1 POWER REQUIREMENTS WMC1



connector at interface level

Figure 1.1 EQUIVALENT CIRCUIT OF POWER SUPPLY INTERFACE FOR WMC1

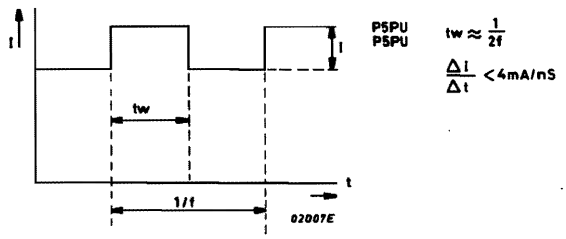
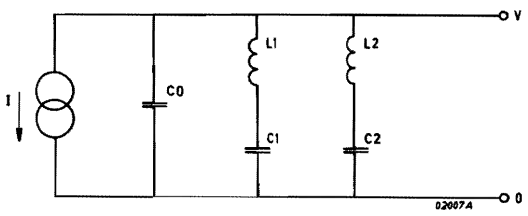


Figure 1.2 WAVEFORM CURRENT AGAINST TIME FOR WMC1

LOGIC NAME	NOM. VOLTAGE	tol%	MAX.AVERAGE CURR.			ΔI max (A)	f max (MC)	Co nF	C1 µF	L1 nH	C2 µF	C2 nH	max. rating V
			ope-rating	stand by	stand by batt.								
P5PU (+5VL)	5.05	4	0.4	0.4	0	0.1	1 (1.5)	1	0.4	0.	33	20	7
P5PU (+5VM)	5.05	4	0.165	0.15	0.15	0.1	1 (1.5)	-	1.4	0.	33	20	7
B12P	12	5	0.65	0.25	0.25	8	2 (3)	-	2.0	0.25	20	3	15

Note: Values in between brackets for "High Speed Version"

Table 1.2 POWER REQUIREMENTS WMB1



Connector at interface level

Figure 1.3 EQUIVALENT CIRCUIT OF POWER SUPPLY INTERFACE FORM WMB1

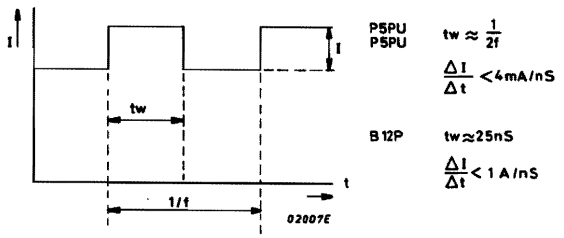


Figure 1.4 WAVEFORM CURRENT AGAINST TIME FOR WMB1

		Memory size (K bytes)							
Mode	Supply	128	256	384	512	640	768	896	1024
Operating	P5PU (+5VL)	2.7	3.1	3.5	3.9	4.3	4.7	5.1	5.5
		(3.1)	(3.5)	(3.9)	(4.3)	(4.7)	(5.1)	(5.5)	(5.9)
	P5PU (+5VM)	1.36	1.53	1.7	1.86	2.03	2.19	2.36	2.52
	B12P (+12VM)	0.65	0.9	1.15	1.4	1.65	1.9	2.15	2.4
Stand by	P5PU	2.7	3.1	3.5	3.9	4.3	4.7	5.1	5.5
		(3.1)	(3.5)	(3.9)	(4.3)	(4.7)	(5.1)	(5.5)	(5.9)
	B5PU	1.35	1.5	1.65	1.8	1.95	2.1	2.25	2.4
	B12P	0.25	0.5	0.75	1.0	1.25	1.5	1.75	2
Stand by	P5PU	-	-	-	-	-	-	-	-
battery	B5PU	1.35	1.5	1.65	1.8	1.95	2.1	2.25	2.4
	B12P	0.25	0.5	0.75	1.0	1.25	1.5	1.75	2

Note: Values in between brackets for "High Speed Version".

Table 1.3 POWER SUPPLY CURRENT MEMORY MODULE

Note: Current Values Given in Amperes

1.3.3 PHYSICAL CHARACTERISTICS

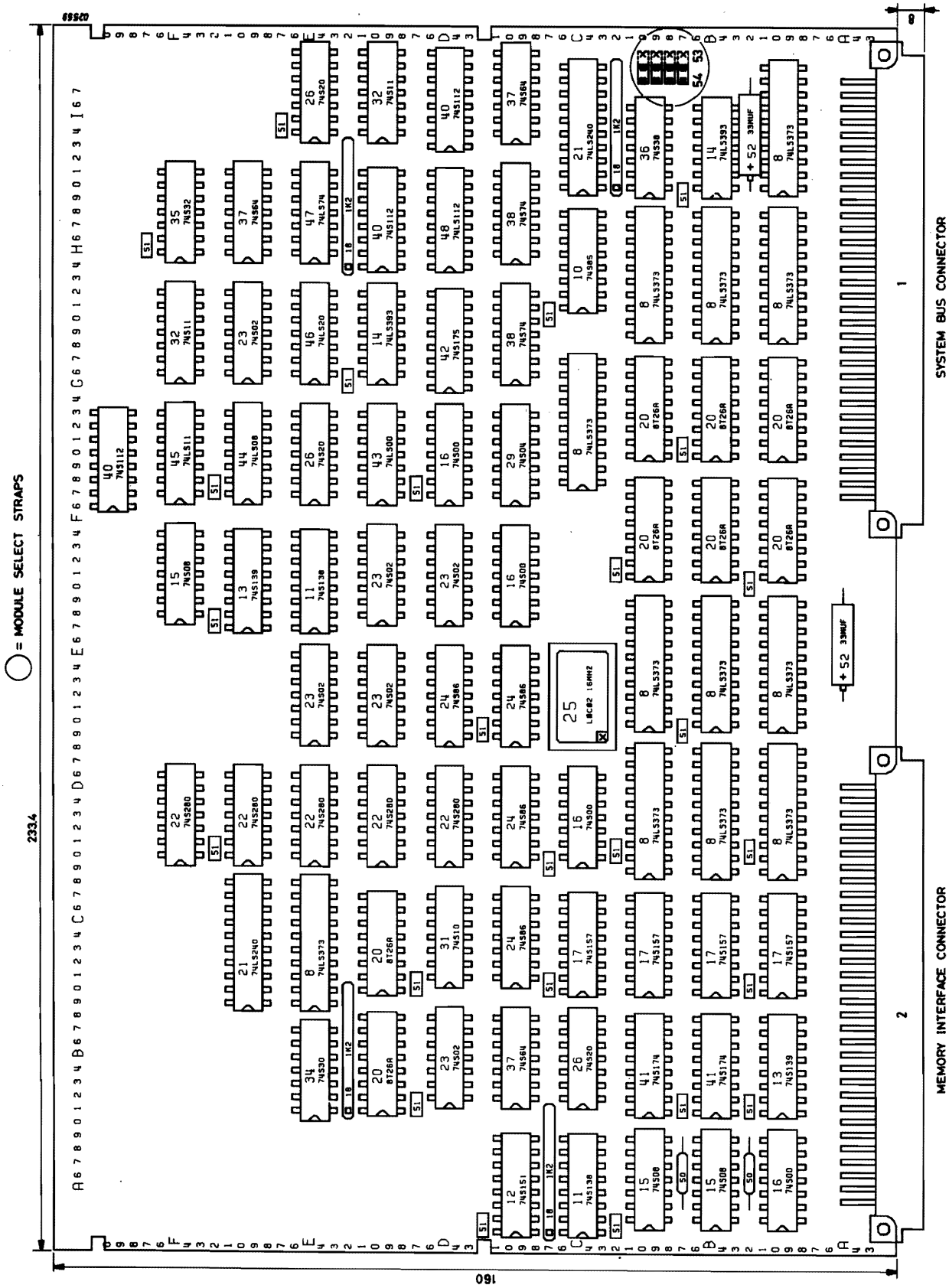


Figure 1.5 CONNECTOR LAYOUT WMC 1

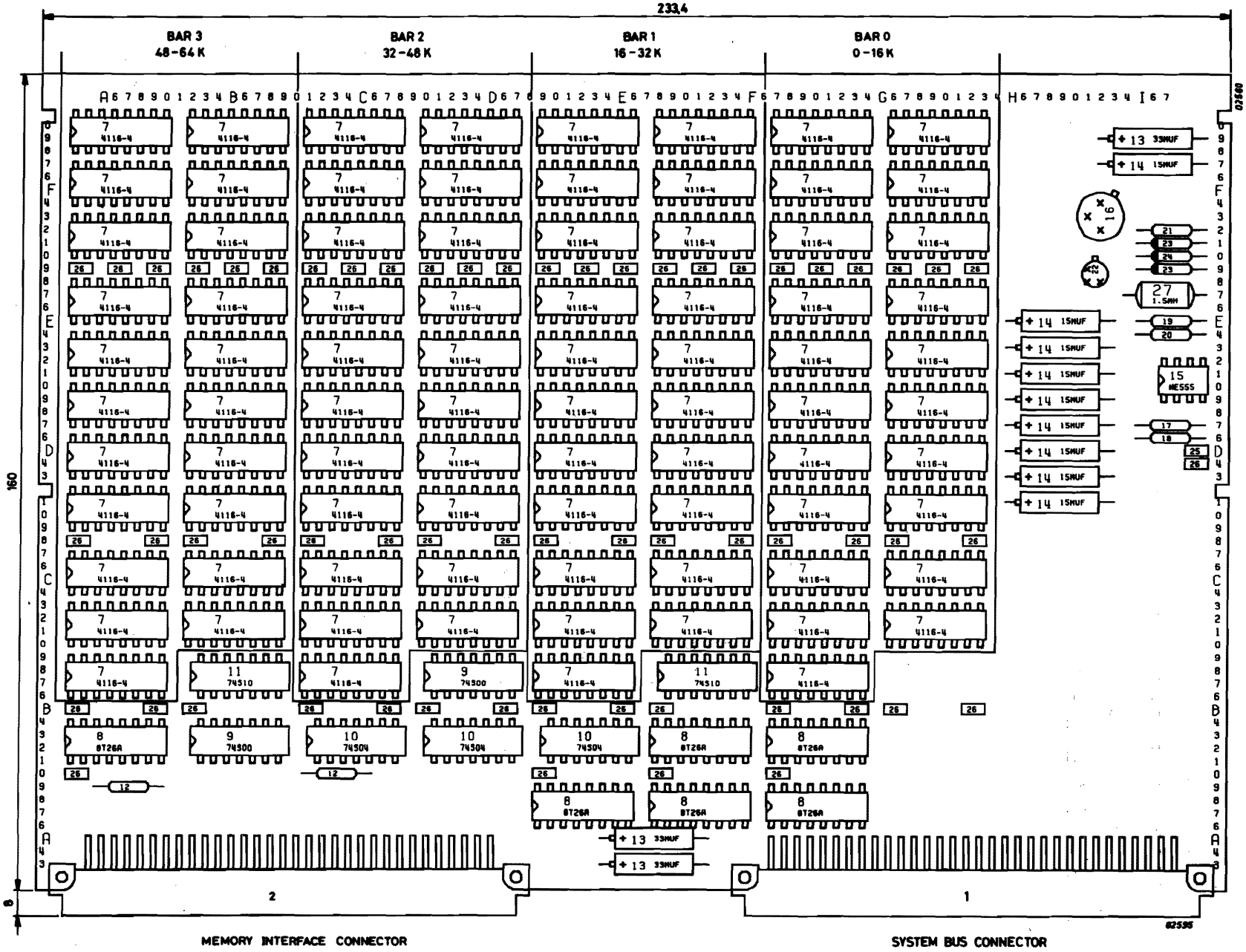


Figure 1.6 CONNECTOR LAYOUT WMB 1

The connectors to the backpanel are 96-pins male connectors. In figure 1.7 the dimensions and pin numbering are indicated.

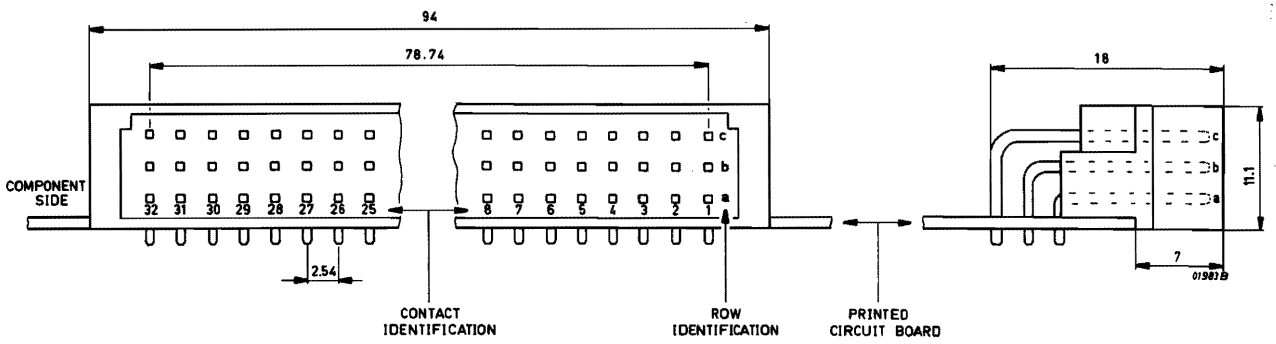


Figure 1.7 BOTTOM VIEW AND SIDE VIEW OF THE BACKPANEL CONNECTORS

CARD	CONNECTOR	TYPE
WMC1	BUS	CON-MP F068-96C
	MEMORY INTERFACE	CON-MP F068-96C
WMB1	BUS	CON-MP F068-96C
	MEMORY INTERFACE	CON-MP F068-64C

Table 1.4 CONNECTOR TYPES

1.3.4 ENVIRONMENTAL CONDITIONS

Operating Conditions:

	TEMPERATURE		REL. HUMIDITY	
	MIN.	MAX.	MIN.	MAX
ABSOLUTE OPERATING LIMITS	5°C	40°C	10%	98%
OPTIMUM OPERATING LIMITS	12°C	32°C	20%	90%

The dynamic limitsΔT = 10°C / 30 minutes

The air velocity between the cards must be more than 1.5 m/sec.

Storage Conditions:
(Packed or unpacked)

TEMPERATURE		REL. HUMIDITY	
MIN.	MAX.	MIN.	MAX.
+3°C	+50°C	10%	90%

The dynamic limitΔT = 10°C / 30 minutes

	PACKED		UNPACKED	
	MIN.	MAX.	MIN.	MAX.
TEMPERATURE	-40°C	+70°C	-40°C	+70°C
REL. HUM.12 HOURS	10%	100%	10%	90%
REL. HUM. 6 WEEKS	10%	98%	10%	90%
REL. HUM. 3 MONTHS	10%	90%	10%	90%

The dynamic limitΔT = 30°C / 5 minutes.

Air Pressure:

	MIN.	MAX.
OPERATING LIMITS	700 mbar	1100 mbar
NON-OPERATING LIMITS	450 mbar	1100 mbar

700 mbar is an altitude of approximately 2250 meters above sea-level.

450 mbar is an altitude of approximately 6300 meters above sea-level.

1.4 INTERFACES

The interfaces of the main memory module can be defined as follows:

1.4.1 - User Interface (Handling of MOS Memory Modules)

1.4.2 - Logical Interface

1.4.3 - Electrical Interface

1.4.4 - Machanical Interface

1.4.1 USER INTERFACE

Note that special care must be taken when handling, repairing or packaging MOS memory modules due to the build-up of static, which may occur and possibly discharge on one pin, thus damaging the device. It is therefore essential to prevent any difference in potential voltage between MOS device and any surface, tool or person with which it may come into contact. The following rules may be helpful:

a) PACKING

MOS circuit boards may be packaged in a metal box, a wooden case, a cardboard box, or conductive plastic, but not in ordinary plastic. These conductive, or semi-conductive, materials prevent static discharge at one point.

b) REPAIRING

It is preferable that all work on MOS devices is carried out on a metal surface, which is in some way connected to ground. All tools and the device should remain on this surface throughout and the personnel must 'discharge' themselves on it before work commences.
All electrical equipment used (e.g. 'scopes, digital voltmeters and the tip of the soldering iron) must be earthed.

c) PERSONNEL

It is advisable for personnel to 'ground' themselves before touching MOS devices, e.g. by touching a metal pipe that is earthed, or at least discharge themselves to the same potential as the working surface before commencing work.

1.4.2 LOGICAL INTERFACES

Four interfaces are applicable under this heading:

a) - UPL Bus
b) - Power Supply
c) - Test Points
d) - Internal Interface

a) - UPL Bus

The logical interface is fully in accordance with the UPL-Bus specification. The table gives a list of the interface signals between the WMC1 card and the system and a short description of their function.

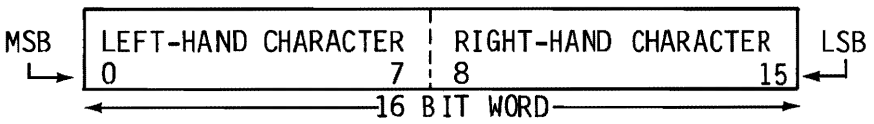
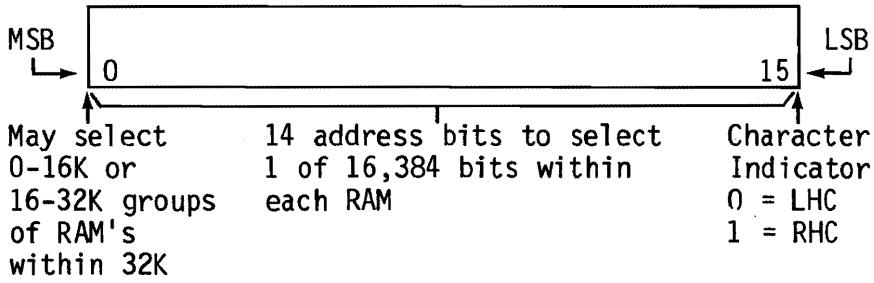
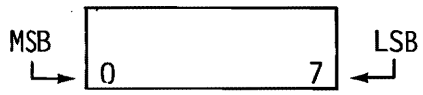
Note that the signals ending in "N" are active (ie, perform their function) when in the "LOW" state ie,logical '0' if they are control signals, and represent the complement of their true value if they are data or address signals.

Note also that control signals (those which cause an immediate action upon their change of state) are always either a logical '0' or a logical '1', whereas data signals are also permitted to adapt to intermediate levels (high Impedance state) when the information is not actually being used in the cycle.

Not connected signals in the UPL Bus are the following:

- BCI
- PWFN
- CLEARN
- TMPN
- TMEN
- ERQN
- BUSRN
- MSN
- BSYN
- RTCH
- BAWOFN
- STOPN
- INCL.

For connector layout and pin assignment see "BUS CONNECTOR SIGNAL TO PIN ASSIGNMENT FOR MEMORY CONTROL CARD WNC1"

UPL BUS SIGNAL	DESCRIPTION
BIO(00-15)N	16 data lines used to transfer data between the memory and other system elements dealing with the interchange of data. 
MAD(00-15)	16 address lines which, during a master-memory exchange, provide addressing signals for the RAM chips, indicate (in character mode) which character is active and may select an "upper" and "lower" 16K within a 32K memory "block". 
MADE(0-7)	8 address extension lines to select memory capacities greater than 32K up to a maximum of 512K words. 
TMRN	A control signal originating in the Master to validate the data on the BIO(00-15)N, WRITE, CHA, MAD(0-7) lines and control the exchange.
TSMN	A control signal originating in the memory to indicate to the master that, in the case of a write cycle, the data has been written into the memory or, if a read cycle, that valid data is now present on the BIO lines.
RSLN	A signal to indicate that the power levels are not in tolerance.
CHA	A control signal transmitted to the memory from the master which has control of the bus to indicate the type of operation as follows: CHA = 0 defines word operation CHA = 1 defines character operation
WRITE	A control signal transmitted from master to memory to indicate the type of operation as follows: WRITE = 0 defines read from memory WRITE = 1 defines write into memory
ACN	A function accepted signal indicating that the function requested by the CPU is accepted, when ACN is LOW.

b) Power Supply

Apart from the actual D.C. voltage supply signals, the only other signal which is applicable is signal RSLN.

When LOW the memory is not accessible and is prepared for operation in 'BATTERY MODE'.

If there is a request (by TMRN) during the transition of RSLN it is possible that the contents of the memory may be damaged.

c) Test Points

Test points are for test purposes only, no connections to these points are permitted during normal operation.

SIGNAL DEFINITIONS

On the memory slave cards

TVBB Test point for the -5V power supply converter.

On the memory control card

TBLRF Input, normal high, a low level blocks refresh requests.

TBLECN Input, normal high, a low level blocks the correction of errors, and also the generation of the error detection signal.

d) Internal Interface (See also figure 1.8)

- Clock signals
  RAS0-1L/R and CAS0-1L/R are timing clock signals to the memory devices, four equal signals of each are given by the control card to the slave cards. The RAS-L/R and CAS-L/R signals are timing related to the MA-L/R signals L to L and R to R.
- Control signals
  EMDO, WE M and RFCYM control signals for respectively Read (Enable Memory Data Out), Write (Write Enable Not) and Refresh cycle, (forbids CAS in refresh cycle). These signals are given to all cards.
- Memory address bits
  MA0-6L/R memory address bits to select one bit in 16K (multiplexed). There is a separate group of addresses for left and right hand memory slave cards.
  One extra address line (MA7L/R) is implemented on the back panel to be upwards compatible with future 64K memory device based designs.

- Bar select signals
  RB0-3 select one out of four bars of memory devices on the memory slave cards.
- Card select signals
  CS0-7N selects one out of eight memory slave cards. Each slave card has its own select-line.
- Memory present signals
  MPR0-7N, these DC signals indicate to the memory control card the presence of a memory card.
- Data I/O
  MIOB00-15 and MIOBS0-S4 bidirectional data lines for data and error correction bits.
- Power supply
  Only ground lines are implemented on the backpanel, all power supply inter connections are through the UPL bus connection. The only galvanic contact between the ground on the backpanel and any other ground point is through the memory cards.

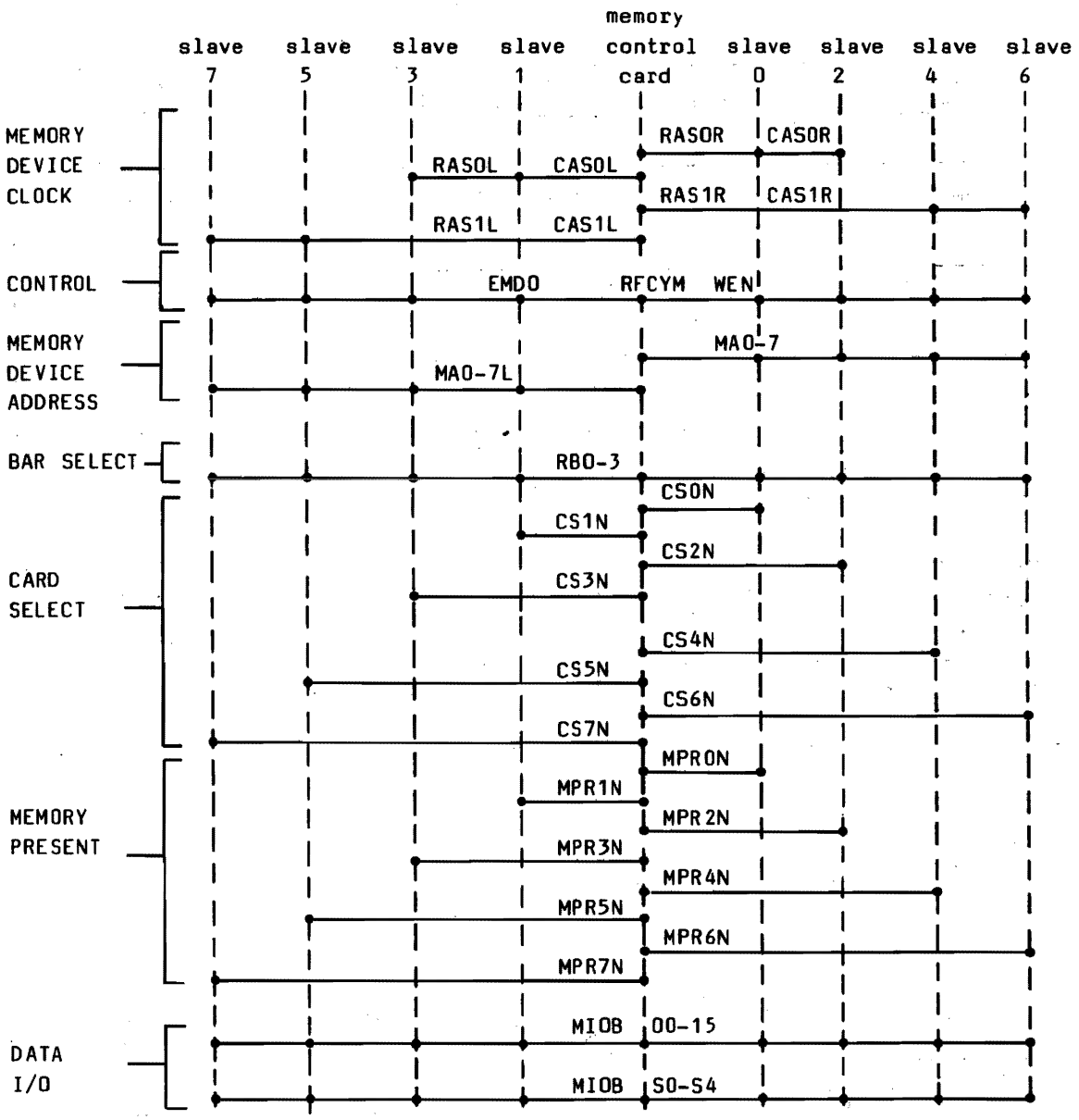


Figure 1.8 INTERNAL INTERFACE (As seen from component side)

1.4.3 ELECTRICAL INTERFACES

SIGNAL NAME	OUTPUT TYPE	LOW LEVEL OUTPUT CURRENT		LOW LEVEL OUTPUT VOLTAGE	HIGH LEVEL OUTPUT CURRENT		CAPACITANCE (PF)		TERMINATING CONFIGURATION	REMARKS
		TRI	OC or TOTEM POLE		TRI	OC	DR.	TX.		
BIO 00-15	Tri or OC	⩽0.4mA at VO=0.5V Tri=off	⩾48mA	⩽0.5V at IOL=48mA	⩽250uA VO=2.4V Tri=off	⩽250uA when VOH=5.5V	⩽15pf	⩽36pf 1)	Pull up at Both Ends of Backpanel by 600Ω± 5% Resistor	
MAD 00-15, MADE 00-07, CHA, WRITE	← ALL CHARACTERISTICS AS SPECIFIED ABOVE →									
TMRN TSMN			⩾60mA	← ALL CHARACTERISTICS AS SPECIFIED IN BIO 00-15 →						
ACN	Tri or OC	⩽0.4mA at VO=0.5V Tri=off	⩾60mA	⩽0.5V at IOL = 60mA	⩽250uA at VO=2.4V Tri=off	⩽250uA VOH=5.5V	⩽15pF	⩽18pf	Pull up at Both Ends of Backpanel by 600Ω± 5% Resistor	
OKO	Totem Pole	N/A	⩾8mA	⩽0.5V at IOL = 8mA	N/A	0.4mA when VOH=2.4V	⩽15pF	N/A	No pull up's	

Table 1.5 DRIVER CHARACTERISTICS FOR SYSTEM BUS

SIGNAL NAME	OUTPUT TYPE	LOW LEVEL INPUT CURRENT	HIGH LEVEL INPUT CURRENT	LOW LEVEL INPUT VOLTAGE	HIGH LEVEL INPUT VOLTAGE	CAPACITANCE (pF)	+Ve THRESHOLD	-Ve THRESHOLD
BIO 00-15	Tri or OC	⩽0.4mA at 0.4V	⩽50uA at 2.7V	⩽0.8V	⩾2V	⩾7pF	-	-
MAD 00-15 MADE 00-07 CHA. WRITE	← ALL CHARACTERISTICS AS ABOVE →							
OKI		<2mA at 0.5V	⩽50uA at 2.7V	<0.8V	>2V	<7pf	-	-
TMRN TSMN		<0.4mA at 0.4V	<50uA at 2.7V	-	-	<7pf	1V-2.1V	0.8-2.1V
RSLN		<0.4mA at 0.5V	<100uA at 2.7V	<0.8V	>2V	<7pf	-	-

Table 1.6 RECEIVER CHARACTERISTICS FOR SYSTEM BUS

1) This is due to a double load on the memory control card for BION signals on the right character.

UPL-BUS INTERFACE FOR MEMORY SLAVE CARD

There is no electrical interface between memory slave card and the UPL bus except OKI-OKO and the power supply.

Used power pins : L, P5PU, B5PU and B12P, for power supply current see Table 1.2.

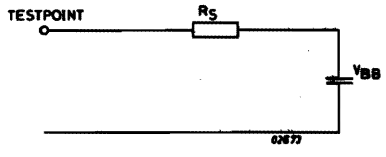
Test Point

- Electrical characteristics inputs

TBLECH	High level input voltage	VIH ⩾ 2V
TBLRF	High level input voltage	VIL ⩽ 0,8V
TBLECH	High level input current	THI ⩽ mA @ VIH = 2.7V
	Low level input current	TIL ⩽ mA @ VIL = 0.4V
TBLRF	High level input current	IIH ⩽ mA @ VIH = 2.7V
	Low level input current	VIL ⩽ mA @ VIL = 0.4V

- Electrical characteristics outputs

TV_{BB}



RS = 1KOhm ± 5%

V_{BB} = 1.75 ⩽ V ⩽ 5.25V

@ B12P ± 5%

1.4.4 MECHANICAL INTERFACE

For connector layout and pin assignments see "BUS CONNECTOR SIGNAL TO PIN ASSIGNMENT".

For Backpanel pin designations see "INTERNAL INTERFACE CONNECTOR".

1.5 APPLICATION NOTES

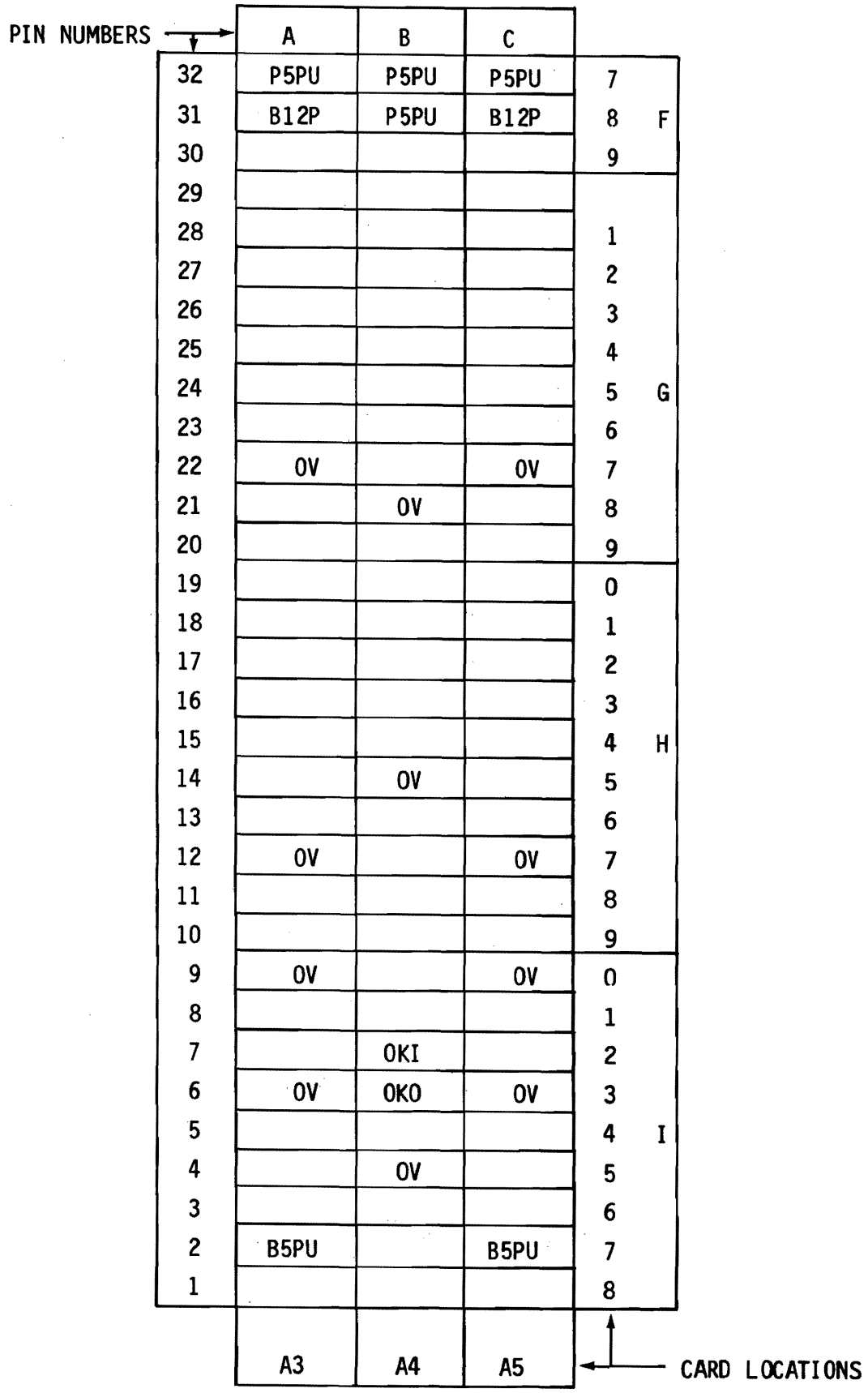
t.b.s.

BUS CONNECTOR SIGNAL TO PIN ASSIGNMENT
FOR MEMORY CONTROL CARD WMC1

PIN NUMBERS →	A	B	C		
32	P5PU	P5PU	P5PU	7	
31		P5PU		8	F
30	BIO07N		BIO15N	9	
29	BIO06N		BIO14N		
28	BIO05N		BIO13N	1	
27	BIO04N		BIO12N	2	
26	BIO03N		BIO11N	3	
25	BIO03N		BIO10N	4	
24	BIO01N		BIO09N	5	G
23	BIO00N		BIO08N	6	
22	0V		0V	7	
21	WRITE	0V	CHA	8	
20	MAD 15	MADE7	MAD 14	9	
19	MAD 13	MADE6	MAD 12	0	
18	MAD 11	MADE5	MAD 10	1	
17	MAD 09	MADE4	MAD 08	2	
16	MAD 07	MADE3	MAD 06	3	
15	MAD 05	MADE2	MAD 04	4	H
14	MAD 03	0V	MAD 02	5	
13	MAD 01	MADE1	MAD 00	6	
12	0V	MADE0	0V	7	
11	TMRN			8	
10	TSMN			9	
9	0V		0V	0	
8	ACN			1	
7	RSLN	OKI		2	
6	0V	OKO	0V	3	
5				4	I
4		0V		5	
3				6	
2	B5PU		B5PU	7	
1				8	
	A3	A4	A5	← CARD LOCATIONS	

Note: OKI/OKO are short circuited on the card.

BUS CONNECTOR SIGNAL TO PIN ASSIGNMENT
FOR MEMORY SLAVE CARD WMB1



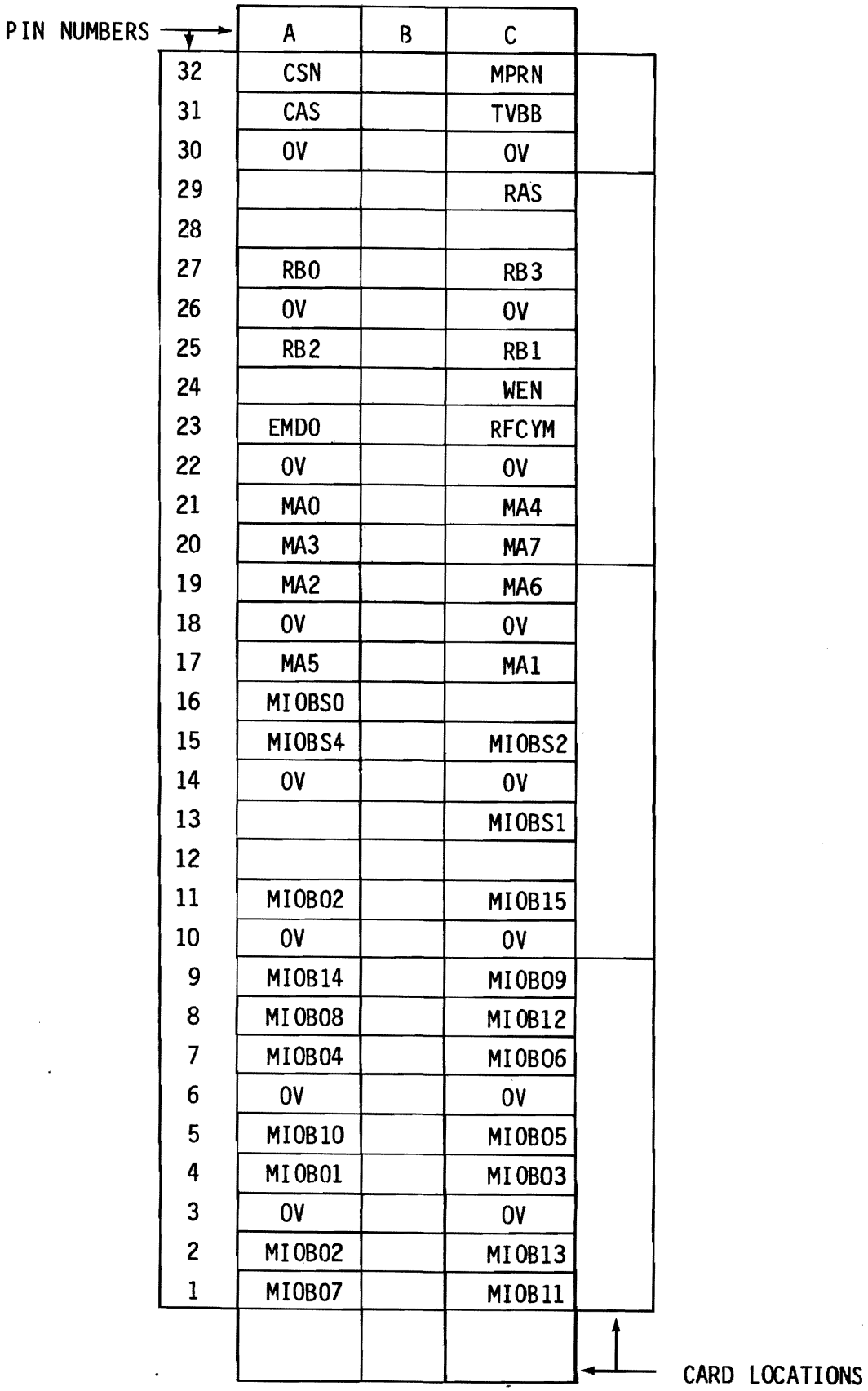
Note: OKI/OKO are short circuited on the card.

MEMORY CONTROL CARD WMC1. INTERNAL INTERFACE CONNECTOR

PIN NUMBERS →	A	B	C
32	CS3N	0V	CS0N
31	CS1N	CS2N	CS7N
30	0V	CS4N	0V
29	CS6N	CS5N	MPR6N
28	MPR7N	0V	MPR4N
27	MPR3N	MPR5N	MPR2N
26	0V	MPR0N	0V
25	MPR1N	CAS0R	CAS1R
24	CAS0L	0V	RAS0R
23	CAS1L	RAS0L	RAS1R
22	0V	RAS1L	0V
21	RB0	RB3	TBLECN
20	RB2	0V	RB1
19	TBLRF		WEN
18	0V	EMD0	0V
17	MA0L	MA0R	RFCYM
16	MA4L	0V	MA4R
15	MA7L	MA8L	MA3R
14	0V	MA7R	0V
13	MA2L	MA2R	MA6R
12	MA6L	0V	MA5R
11	MA5L	MA1L	MA1R
10	0V	MI0BS0	0V
9	MI0BS4	MI0BS1	MI0BS2
8	MI0B02	0V	MI0BS3
7	MI0B04	MI0B15	MI0B06
6	0V	MI0B14	0V
5	MI0B10	MI0B09	MI0B05
4	MI0B01	0V	MI0B03
3	0V	MI0B08	0V
2	MI0B00	MI0B12	MI0B13
1	MI0B07		MI0B11

← CARD LOCATIONS

MEMORY SLAVE CARD WMB1. INTERNAL INTERFACE CONNECTOR



PIN NUMBERS	A	B	C
32	CSN		MPRN
31	CAS		TVBB
30	0V		0V
29			RAS
28			
27	RB0		RB3
26	0V		0V
25	RB2		RB1
24			WEN
23	EMD0		RFCYM
22	0V		0V
21	MA0		MA4
20	MA3		MA7
19	MA2		MA6
18	0V		0V
17	MA5		MA1
16	MI0BS0		
15	MI0BS4		MI0BS2
14	0V		0V
13			MI0BS1
12			
11	MI0B02		MI0B15
10	0V		0V
9	MI0B14		MI0B09
8	MI0B08		MI0B12
7	MI0B04		MI0B06
6	0V		0V
5	MI0B10		MI0B05
4	MI0B01		MI0B03
3	0V		0V
2	MI0B02		MI0B13
1	MI0B07		MI0B11

CARD LOCATIONS

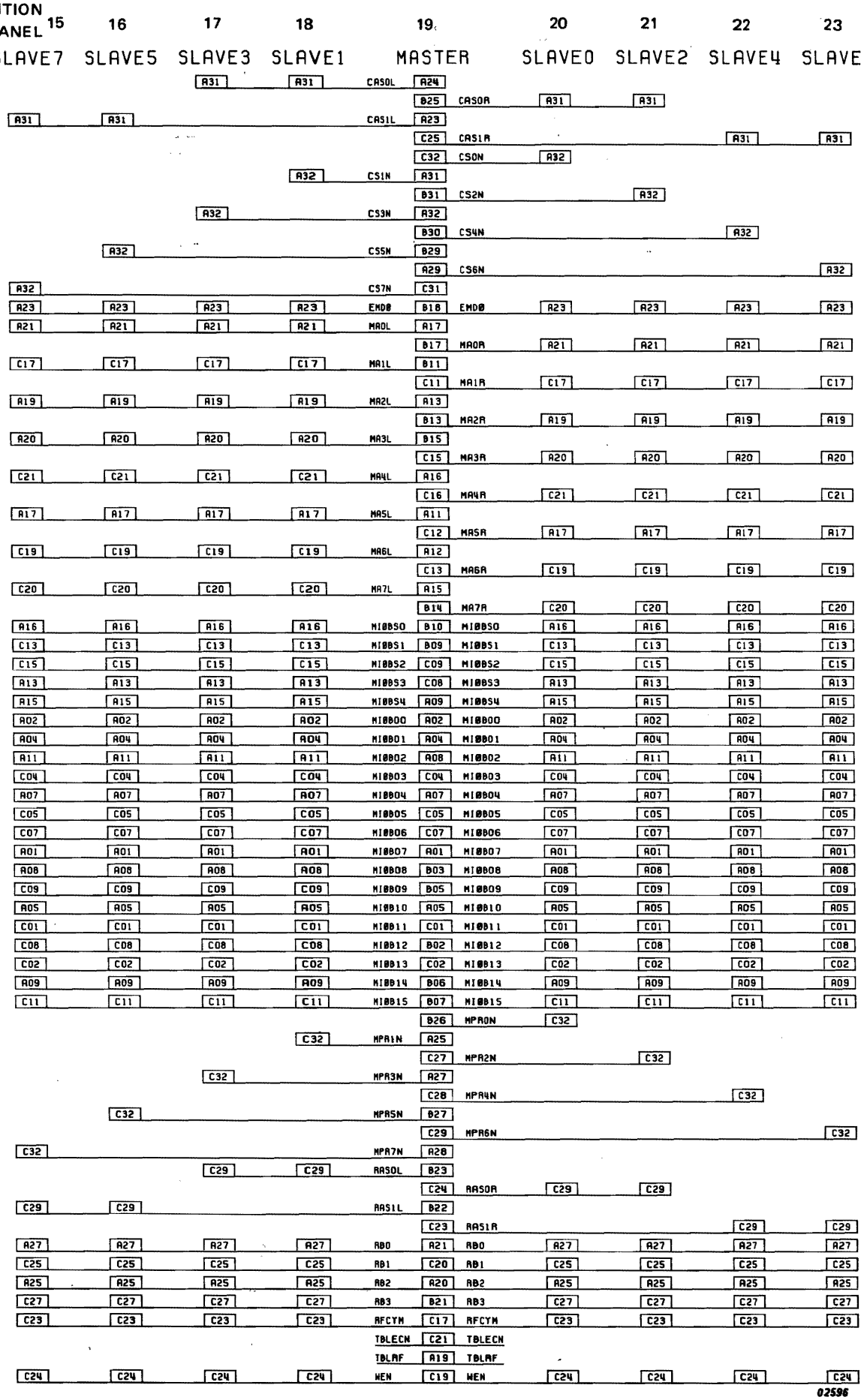


Table 1.7 BACKPANEL PIN DESIGNATIONS FOR INTERNAL INTERFACE (AS SEEN FROM THE SOLDER SIDE)

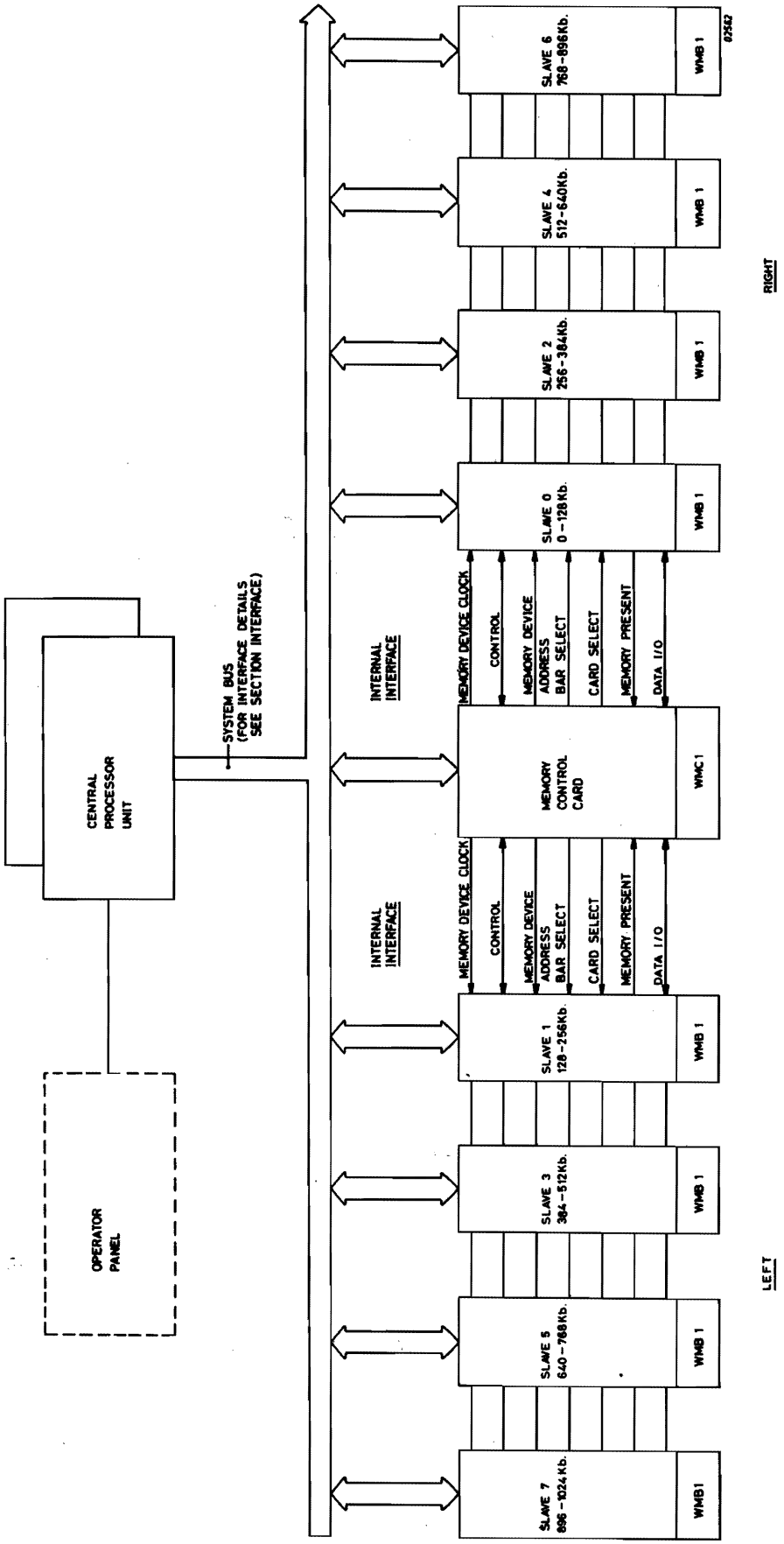


Figure 1.9 1MBYTE MEMORY IN SYSTEM APPLICATION P4500

1.6 INSTALLATION DATA

1.6.1 CARD INSTALLATION (Refer to figure 1.10)

The location of the memory control card and successive memory slave cards for increasing memory capacity is fixed by the wiring on the backpanel.

There are no straps or bridges whatsoever on the special backpanel, memory control card or memory slave cards for adjusting the memory capacity within a 1M byte module.

For a required memory capacity the cards must be inserted in the backpanel as given in the table below. (The table 1.8 shows a complete UPL bus system.)

Backpanel loc	15	16	17	18	19	20	21	22	23
Card type	WMB1	WMB1	WMB1	WMB1	WMC1	WMB1	WMB1	WMB1	WMB1
Card select no	7	5	3	1		0	2	4	6
Mem size (byte)									
0 - 128K					x	x			
0 - 256K				x	x	x			
0 - 384K				x	x	x	x		
0 - 512			x	x	x	x	x		
0 - 640			x	x	x	x	x	x	
0 - 768		x	x	x	x	x	x	x	
0 - 896		x	x	x	x	x	x	x	x
0 - 1M	x	x	x	x	x	x	x	x	x

Table 1.8 MEMORY CAPACITY DETERMINATION

From a hardware point of view it is not necessary to have the memory slave cards ranked together; in this case gaps in the memory area of at least 128K bytes will occur.
These gaps may be filled with other memory cards e.g.
2 x 64 byte memory cards with E.C.

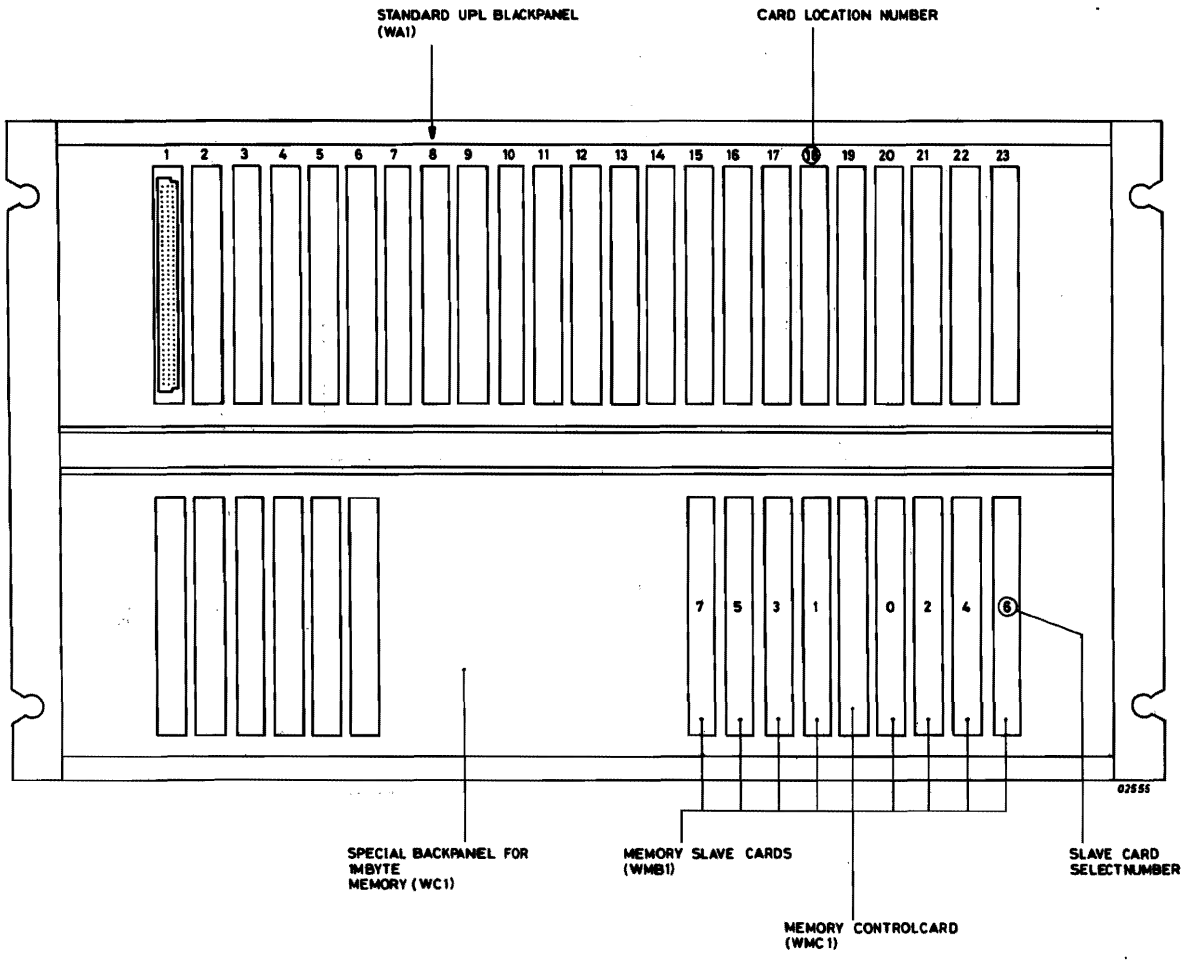


Figure 1.10 BACKPANEL FOR 1M BYTE MEMORY MODULE P4500

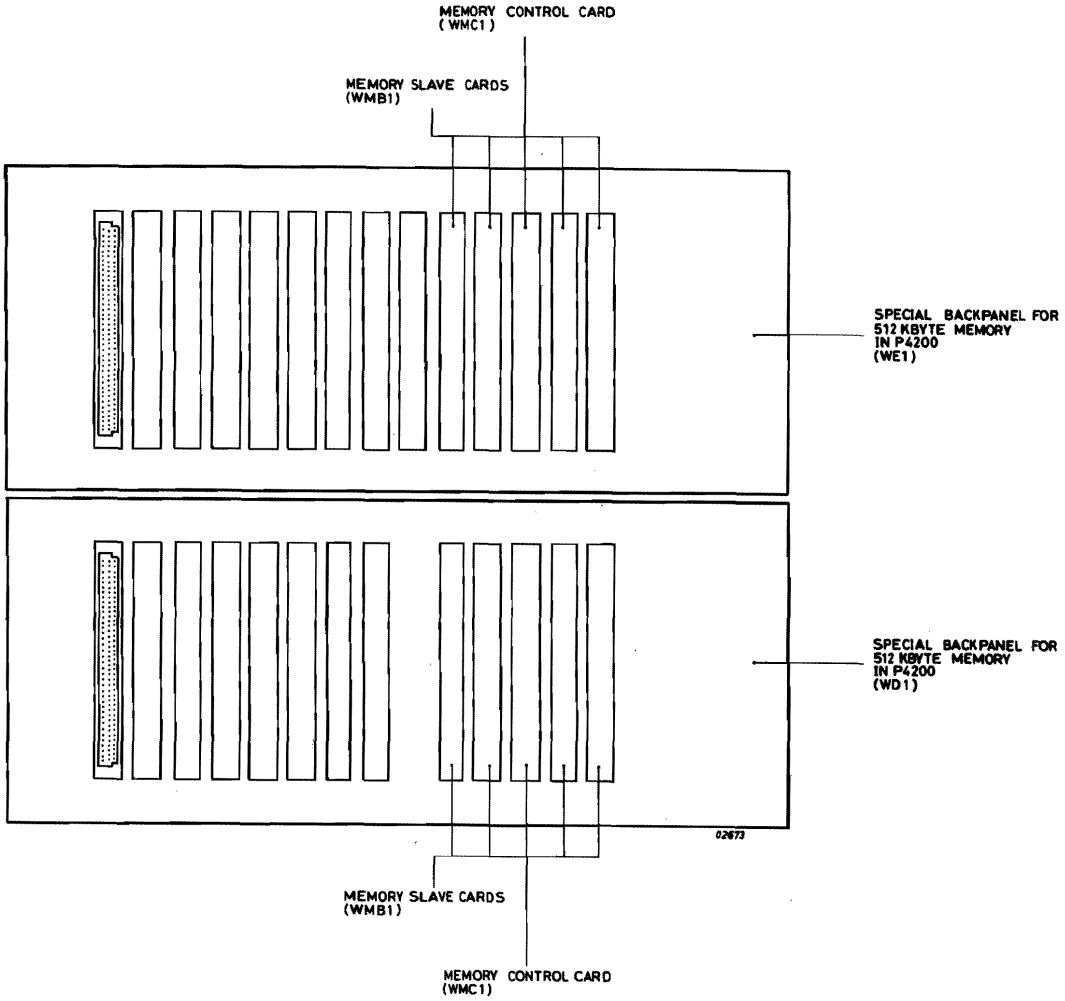


Figure 1.11 BACKPANEL FOR 512K BYTE MEMORY MODULE P4500S

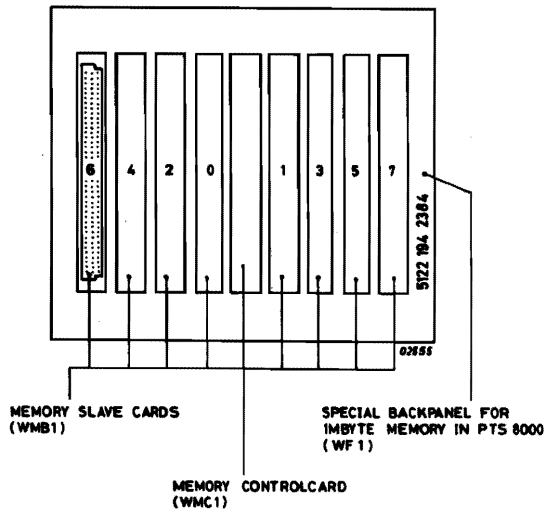


Figure 1.12 BACKPANEL FOR 1M BYTE MEMORY MODULE PTS8000

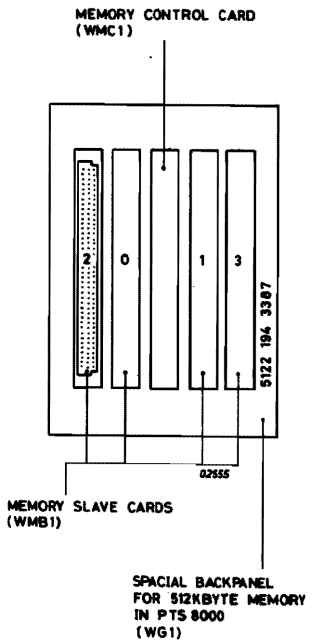


Figure 1.13 BACKPANEL FOR 512K BYTE MEMORY MODULE PTS8000

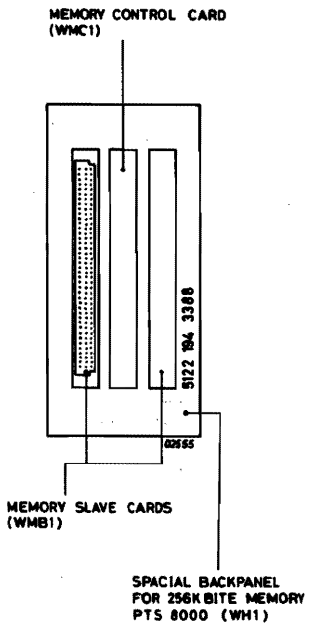


Figure 1.14 BACKPANEL FOR 256K BYTE MEMORY MODULE PTS8000

1.6.2 MODULE SELECT STRAPS

The module select address is a binary number installed by 4 straps (strapnr. 0 - 3, nr. 0 most significant.

By means of these straps addresses up to 16M bytes (8M words) can be handled in multiples of 1M bytes (512K words).

The relation between module select and strap location is listed below in Table 1.9.

Module select address	Memory array	Location of the strap			
		0	1	2	3
'0' X	0M - 1M	I8B7	I8B8	I8B9	I8C0 **
'1' X	1M - 2M	I8B7	I8B8	I8B9	I9C0
'2' X	2M - 3M	I8B7	I8B8	I9B9	I8C0
'3' X	3M - 4M	I8B7	I8B8	I9B9	I9C0
'4' X	4M - 5M	I8B9	I9B8	I8B9	I8C0
'5' X	5M - 6M	I8B7	I9B8	I8B9	I9C0
'6' X	6M - 7M	I8B7	I9B8	I9B9	I8C0
'7' X	7M - 8M	I8B7	I9B8	I9B9	I9C0
'8' X	8M - 9M	I9B7	I8B8	I8B9	I8C0
'9' X	9M - 10M	I9B7	I8B8	I8B9	I9C0
'A' X	10M - 11M	I9B7	I8B8	I9B9	I8C0
'B' X	11M - 12M	I9B7	I8B8	I9B9	I9C0
'C' X	12M - 13M	I9B7	I9B8	I8B9	I8C0
'D' X	13M - 14M	I9B7	I9B8	I8B9	I9C0
'E' X	14M - 15M	I9B7	I9B8	I9B9	I8C0
'F' X	15M - 16M	I9B7	I9B8	I9B9	I9C0

X Hexadecimal address number

** Manufacturer position of straps

Table 1.9 STRAP POSITIONING TABLE

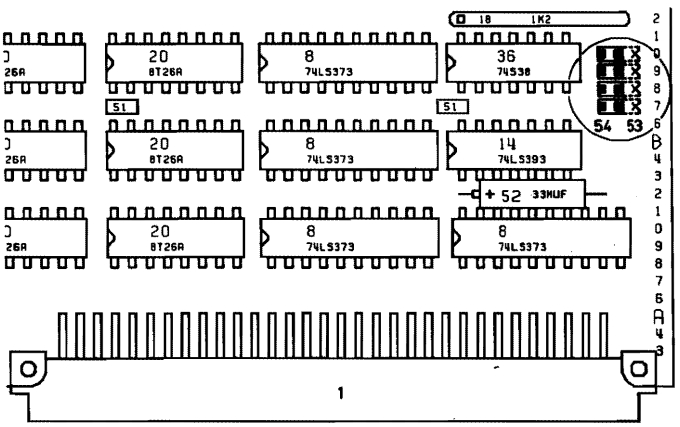


Figure 1.15 MODULE SELECT STRAPS

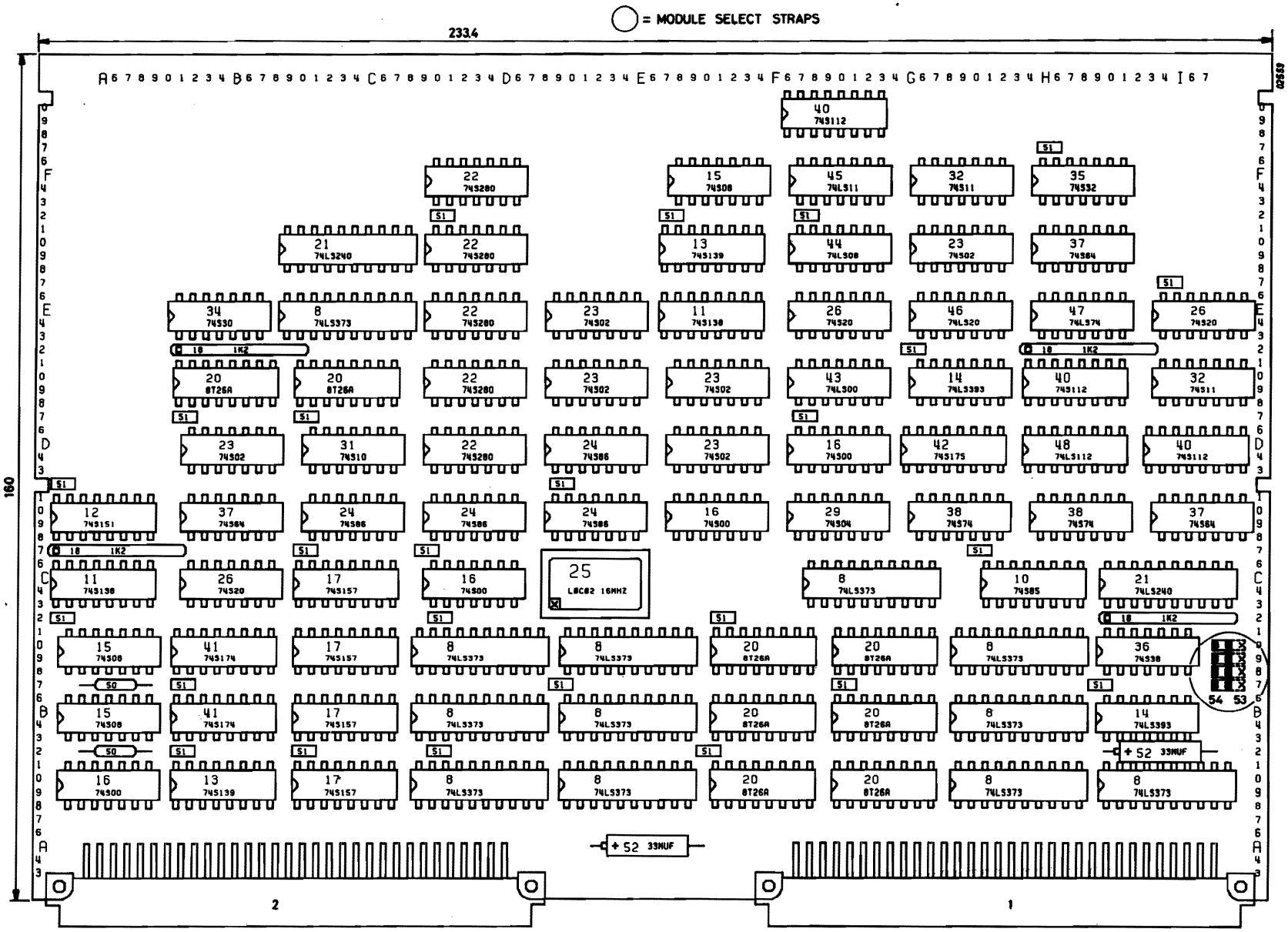
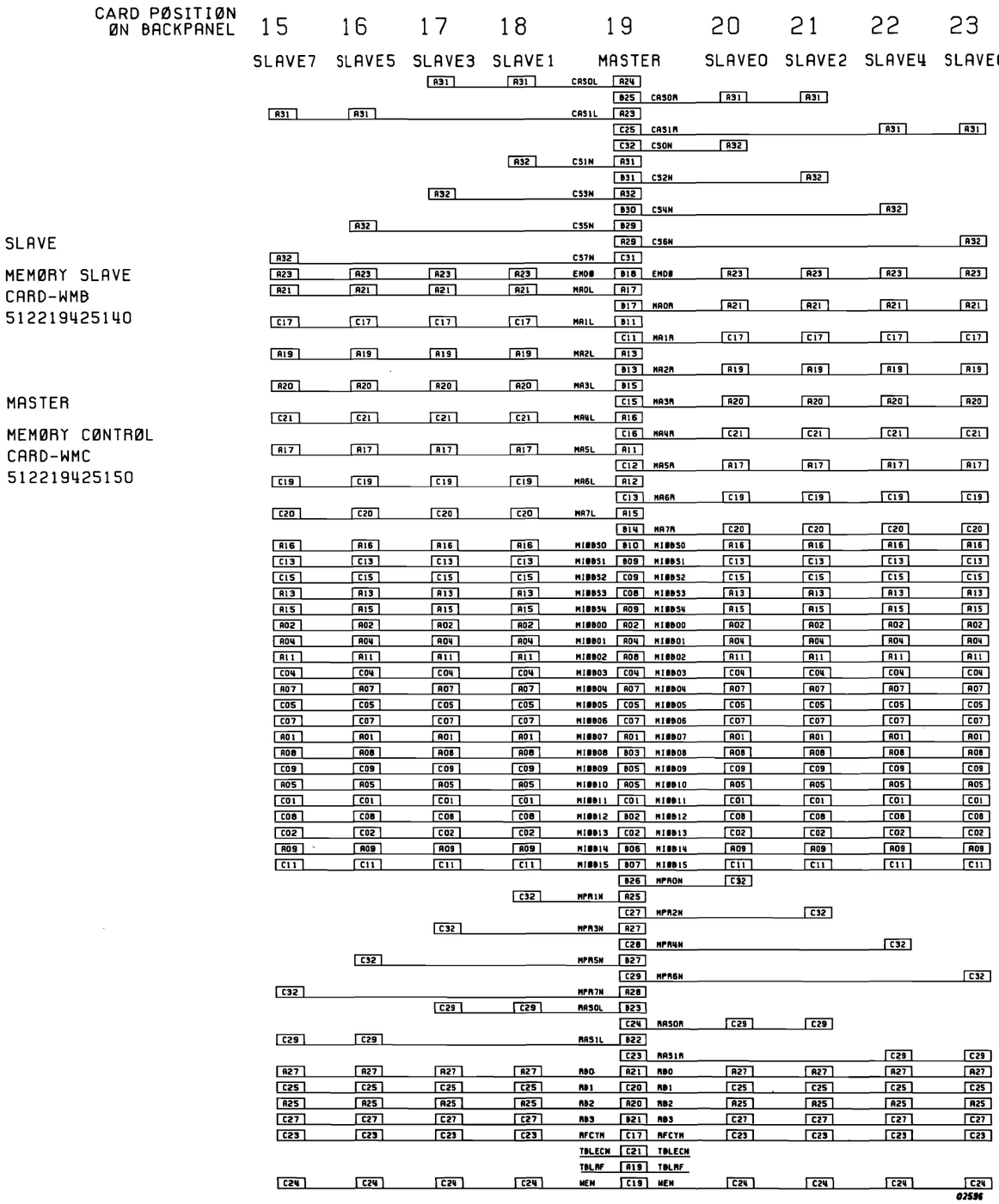
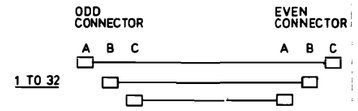


Figure 1.16 STRAP POSITIONS WMC1





FROM CARD POSITION ON BACKPANEL 1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14, ARE THE LOGIC POINTS CONNECTED AS SHOWN.

Figure 1.17 BACKPANEL INTERCONNECTIONS FOR P4500 1M BYTE

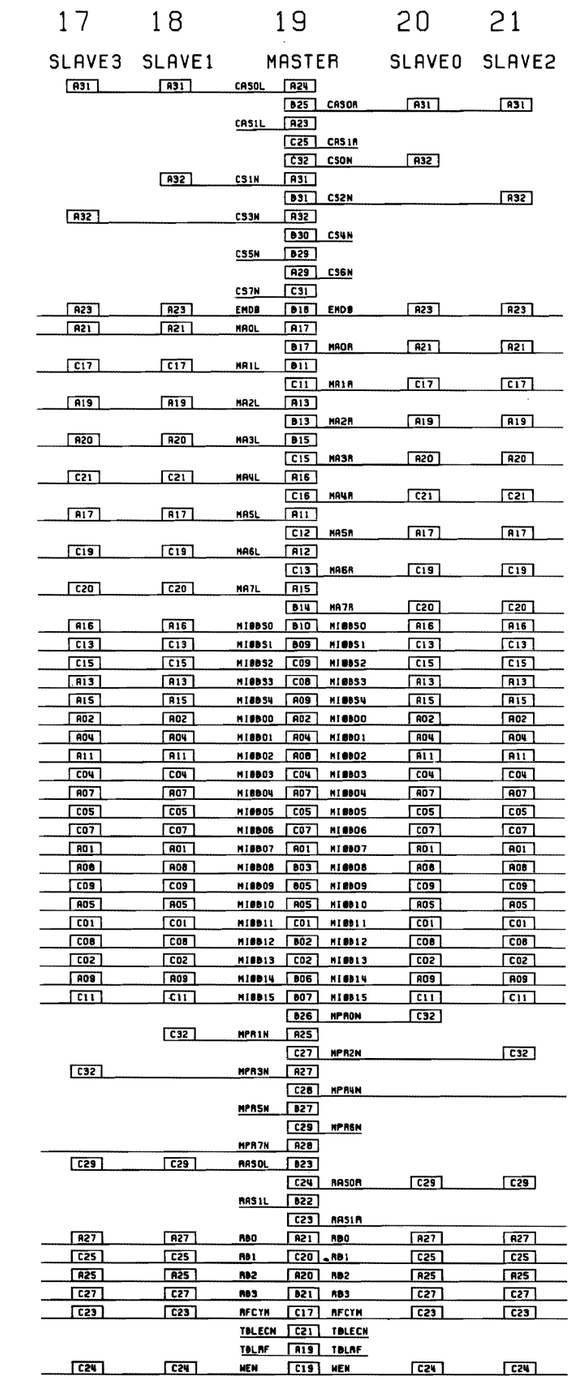
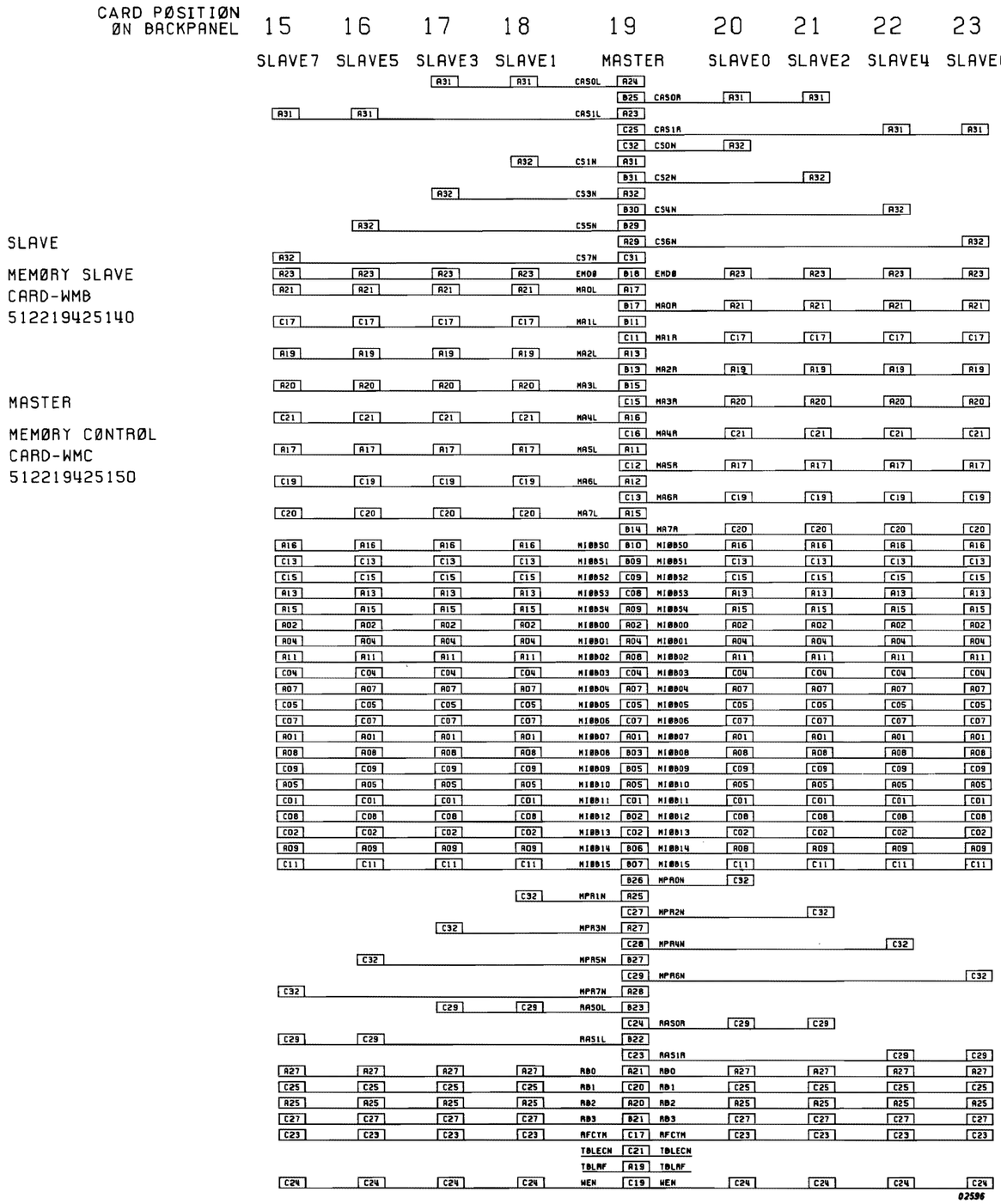
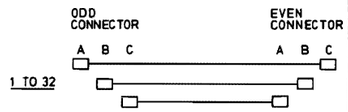


Figure 1.18 BACKPANEL INTERCONNECTIONS FOR P4500 SMALL 512K BYTE



02596



FROM CARD POSITION ON BACKPANEL 1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14, ARE THE LOGIC POINTS CONNECTED AS SHOWN.

Figure 1.19 BACKPANEL INTERCONNECTIONS FOR PTS 8000, 1M BYTE

17	18		19		20	21
SLAVE3	SLAVE1		MASTER		SLAVE0	SLAVE2
A31	A31	CA50L	A24			
			B25	CA50R	A31	A31
		CA51L	A23			
			C25	CA51R		
			C32	CS0N	A32	
	A32	CS1N	A31			
			B31	CS2N		A32
A32		CS3N	A32			
			B30	CS4N		
		CS5N	B29			
			A29	CS6N		
		CS7N	C31			
A23	A23	EMD0	B18	EMD0	A23	A23
A21	A21	MA0L	A17			
			B17	MA0R	A21	A21
C17	C17	MA1L	B11			
			C11	MA1R	C17	C17
A19	A19	MA2L	A13			
			B13	MA2R	A19	A19
A20	A20	MA3L	B15			
			C15	MA3R	A20	A20
C21	C21	MA4L	A16			
			C16	MA4R	C21	C21
A17	A17	MA5L	A11			
			C12	MA5R	A17	A17
C19	C19	MA6L	A12			
			C13	MA6R	C19	C19
C20	C20	MA7L	A15			
			B14	MA7R	C20	C20
A16	A16	MI0B50	B10	MI0B50	A16	A16
C13	C13	MI0B51	B09	MI0B51	C13	C13
C15	C15	MI0B52	C09	MI0B52	C15	C15
A13	A13	MI0B53	C08	MI0B53	A13	A13
A15	A15	MI0B54	A09	MI0B54	A15	A15
A02	A02	MI0B00	A02	MI0B00	A02	A02
A04	A04	MI0B01	A04	MI0B01	A04	A04
A11	A11	MI0B02	A08	MI0B02	A11	A11
C04	C04	MI0B03	C04	MI0B03	C04	C04
A07	A07	MI0B04	A07	MI0B04	A07	A07
C05	C05	MI0B05	C05	MI0B05	C05	C05
C07	C07	MI0B06	C07	MI0B06	C07	C07
A01	A01	MI0B07	A01	MI0B07	A01	A01
A08	A08	MI0B08	B03	MI0B08	A08	A08
C09	C09	MI0B09	B05	MI0B09	C09	C09
A05	A05	MI0B10	A05	MI0B10	A05	A05
C01	C01	MI0B11	C01	MI0B11	C01	C01
C08	C08	MI0B12	B02	MI0B12	C08	C08
C02	C02	MI0B13	C02	MI0B13	C02	C02
A09	A09	MI0B14	B06	MI0B14	A09	A09
C11	C11	MI0B15	B07	MI0B15	C11	C11
			B26	MPA0N	C32	
	C32	MPA1N	A25			
			C27	MPA2N		C32
C32		MPA3N	A27			
			C28	MPA4N		
		MPA5N	B27			
			C29	MPA6N		
		MPA7N	A28			
C29	C29	MA5OL	B23			
			C24	MA5OR	C29	C29
		MA51L	B22			
			C23	MA51R		
A27	A27	AB0	A21	AB0	A27	A27
C25	C25	AB1	C20	AB1	C25	C25
A25	A25	AB2	A20	AB2	A25	A25
C27	C27	AB3	B21	AB3	C27	C27
C23	C23	AFCYM	C17	AFCYM	C23	C23
		TBLECN	C21	TBLECN		
		TBLAF	A19	TBLAF		
C24	C24	WEN	C19	WEN	C24	C24

Figure 1.20 BACKPANEL INTERCONNECTIONS FOR PTS 8000, 512K BYTES

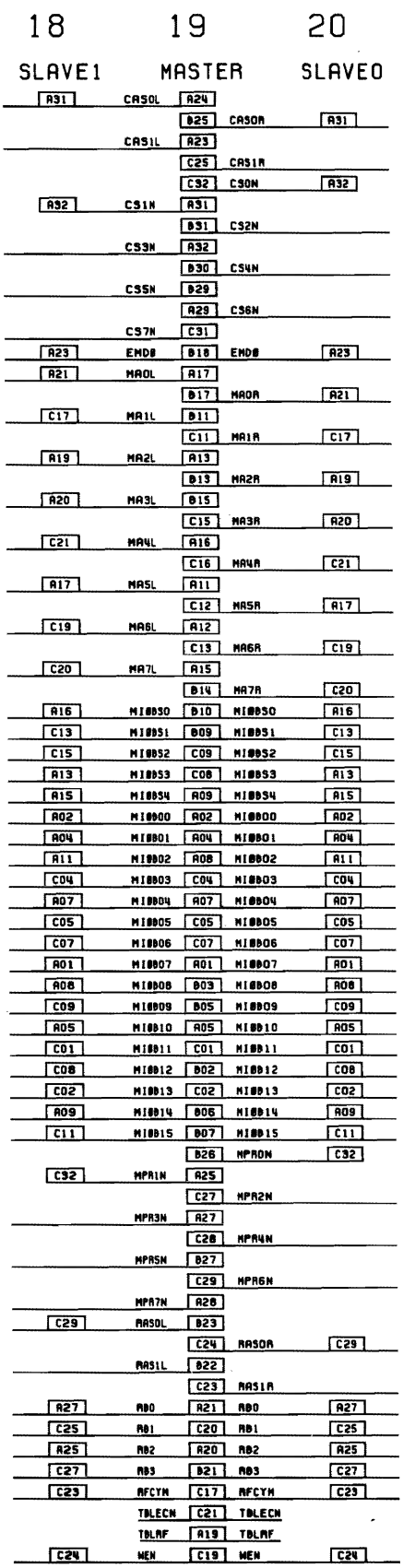


Figure 1.21 BACKPANEL INTERCONNECTIONS FOR PTS 8000, 256K BYTES

2 FUNCTIONAL DESCRIPTION

LIST OF ILLUSTRATIONS

LIST OF TABLES

2.1 GENERAL

The memory block diagram (figure 2.1) and the description is given for a complete module; 8 memory slave cards, one memory control card and a backpanel. The 8 memory slave cards in the block diagram are drawn in the same sequence as they are mounted in the backpanel.

The location of the memory control card is given by a dashed line in the middle of the memory slave cards.
The functional position of the memory control card is between the memory slave cards and the UPL bus. The interface between the memory control card and the slave cards is via the memory backpanel.

2.2 MEMORY ARRAY

The complete memory module is organized as 8 times 64K16 bit words comprising entirely of dynamic MOS read, write memory device of the 4116 (Mostek) type.
For error detection and correction 5 bits are added to the 16 data bits so the memory is actually 512K21 bits. (16 + 5).

The memory array on each memory slave card consists of 4 bars each of 21 memory devices.

Read and Write cycles are always carried out for all 21 bits, independant of whether word or character mode is used. The memory devices have, in order to allow the smallest possible package, the 14 address bits necessary to choose one out of 16.384 bits multiplexed into 7 address inputs. The two multiplexed address words are latched into the RAM with two clocks Row Address Strobe (RAS) and Column Address Strobe (CAS).
Due to the dynamic nature of the memory devices data must be restored (refreshed) by selecting each row within a 2mSec period.

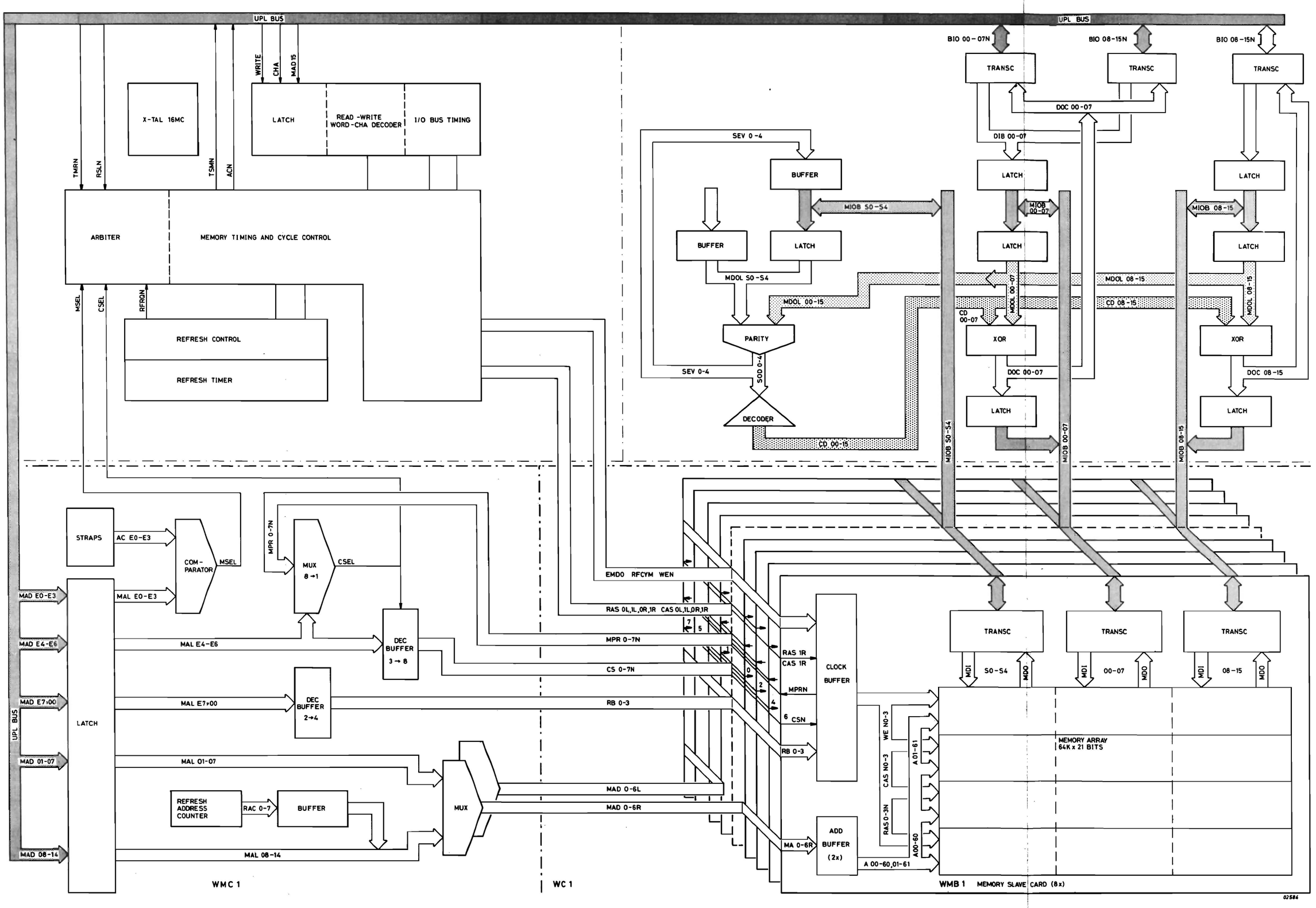
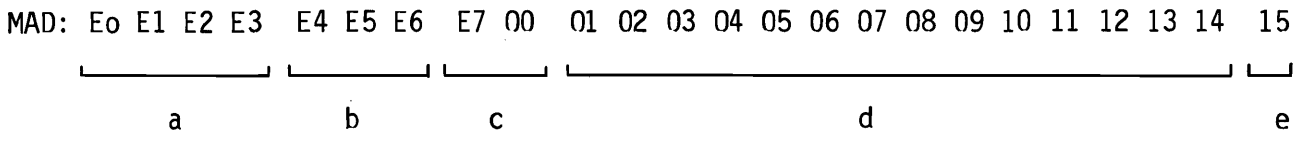


Figure 2.1 MEMORY MODULE BLOCK DIAGRAM

2.3 ADDRESSING

There is a total of 24 bits used for addressing which are organized as follows:



- a) Module select addresses. This part of the address string is used to give the complete memory module an allocation between 0 - 16M bytes in steps of 1M bytes, (see also Installation section).

- b) MADE4 to MADE6. Used for selection of one out of the eight memory slave cards.
  When selecting a present memory slave card, indicated by MPR-N (Memory Present) low, the signal CSEL will enable both the memory cycle and the CS-N signal (Card Select Not) to the memory slave card.
  In case of refresh, the card select decoding is overruled and all cards are selected simultanously.

- c) MADE7, MAD00 . Used to select one out of four of the memory device bars on a slave card by means of the RB0-3 signals (Ras . Bar). In case of refresh all bars will be selected simultanously.

- d) MAD01 to MAD14. Memory device address. Used for selecting one out of 16.384 memory element within a memory device.
  These address lines (14) are multiplexed into two 7 bit address words as required by the memory devices. For buffering and timing reasons the left and right hand memory slave cards have their own multiplexors on the memory control card. (MA-L, MA-R = Memory Address Left, Right).
  During a refresh cycle, the least significant memory device addresses are suppressed and an internally generated address is offered to the memory devices.
  This internally generated address (refresh address) is increased by one at the end of each refresh cycle to a value of 128 (number of rows within one memory device).
- e) MAD15, Character pointer. It will be used in character mode only MAD15 indicates if the least or most significant octad (character) of the memory is directed to the least significant group of BIO-N lines (BIO08-15N).

2.4 DATA I/O

2.4.1 TYPES OF TRANSFERS

There are six possible types of transfer indicated by a combination of WRITE, CHA and MAD15 signals as illustrated in the table below.

WRITE	CHA	MAD15	OPERATION
1	0	Don't care	The 16 bit word on BIO(00-15)N is written at the given address.
1	1	0	The right-hand character on BIO(8-15)N is written into the left character position of the given address.
1	1	1	The right-hand character on BIO(8-15)N is written into the right character position of the given address.
0	0	Don't care	The 16 bit word is read out onto BIO(00-15)N
0	1	0	The left-hand character is read out onto the right character position on BIO(8-15)N.
0	1	1	The right-hand character is read out onto the right character position on BIO(8-15)N.

Table 2.1 CYCLE MODE CONTROL SIGNALS

These various types of transfer are laid out in simplified form in figure 2.2 'SIMPLIFIED DATA TRANSFER'.

Note that a memory cycle always reads or writes a complete 16 Bit word and also that all character transfers to and from memory is via BI008-15N.

- Read Word

  A word is read from the memory array and is routed directly through latches (LAT) 3 and 4, exclusive or (XOR) and TRansceiver to the BIO...N lines while the decoder output to the XOR's is disabled.

  Data and S bits are offered to the parity and decoder circuits, which checks for data error (single bit error). If no error is detected, the decoder stays disabled, and Data out is stable. If there is an error the decoder is enabled and the failing data corrected. The data on BIO-N lines is thus valid later on in the cycle causing the complete cycle to be stretched.

- Read Character (Left or Right)

  A left or right character is read as in a Read Word cycle except that only the data from the selected character of the memory word is presented to the Right character (least significant octad) of the BIO...N lines.

- Write Word

  Data on the BIO...N lines is routed through Transceivers 1, 2 and Latches 1, 2 to the memory array and via Latches 3, 4 to the parity circuit. The parity circuit generates the appropriate error correction code which is written, along with the BIO...N data, into the memory array.

- Write Character (Left or Right)

  Because error correction bits are derived from a 21 bit word, a complete word must be made available to the parity circuit.

  To fulfill this requirement the old memory data is read first, corrected and latched in latch 5 and 6, then the new character on the BIO...N lines and the complementary old character (stored in the latch) are offered to the memory and the parity circuit as in a normal write cycle.

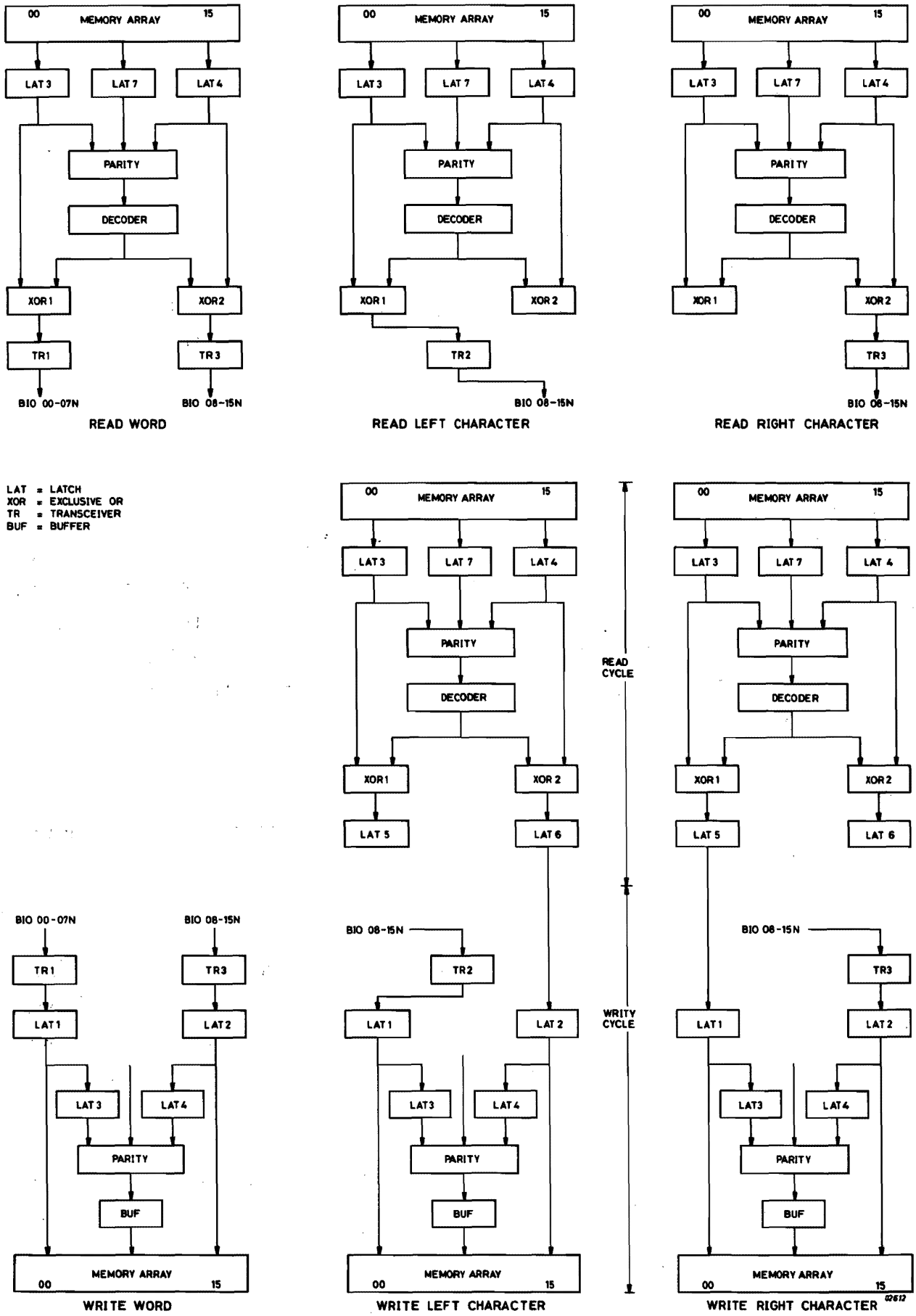


Figure 2.2. SIMPLIFIED DATA TRANSFER MODES

2.5 CONTROL AND TIMING

Within this block the following functions are performed.

- 2.5.1 Arbiter
- 2.5.2 Refresh Control and Timer
- 2.5.3 Memory Timer
- 2.5.4 Memory Cycle Mode Control

2.5.1 ARBITER

The Arbiter will choose between external requests (TMRN) and internal refresh requests (RFRQ). It also synchronizes the external requests with the internal clock oscillator (X-tal 16mc).

2.5.2 REFRESH CONTROL AND TIMER

The refresh circuitry which is necessary due to the dynamic nature of the memory devices consists of two parts.
The Refresh timer has a period time of 15 µsec during which one refresh cycle must take place in order to refresh all 128 rows in a memory device within 2 ms. The refresh control logic will request either a "hidden" or "automatic" refresh cycle and also execute all control functions required during a cycle.
At the end of the refresh cycle the refresh control logic will ensure that the refresh address generator or counter is incremented.

2.5.3 MEMORY TIMER

The memory timer is the general timing generator from which all cycle timing signals are derived.

2.5.4 MEMORY CYCLE MODE CONTROL

As previously mentioned three input signals WRITE, CHA and MAD15 indicate the type of transfer to be performed. These three signals are latched in and decoded. The decoded outputs in conjunction with the memory timer will create all the timing signals necessary to control the data I/O bus. (I/O Bus Timing Control).

These timing signals are also used for cycle control ie. Read, Write Cycle and Word or Character mode transfer.

3 DETAILED DESCRIPTION

LIST OF ILLUSTRATIONS

LIST OF TABLES

3.1 GENERAL

In this subsection a logical description will be given for the various parts of the memory module, as used in P4500. In section 3.10, some information is given for the high speed version as used in PTS8000. The description will be given as far as possible, for a complete module.
A complete module consists of the following items:

- Memory control card; WMC.
  As can be seen in the block diagram this card forms the interface between the UPL bus and the memory slave cards.
  All the logic for address, data, error-correcting and timing has been concentrated on this card in order to reduce the number of TTL's in the memory module.

- Memory slave card; WMB1 (8x)
  Each slave card contains a part of the memory array, some buffer logic and a +12V to -5V converter for the memory devices.
  Except for OKI-OKO and power supply the memory slave card has no interface with the UPL bus.

- Memory interface backpanel
  The backpanel forms the interface between the memory control card and the memory slave cards. Due to a unique wiring for card select and memory present, each card in the memory module has its own predetermined slot.

3.2 MEMORY ARRAY (See figures 3.1 and 3.2)

As mentioned previously the complete memory array is divided on 8 memory slave cards, each card containing 4 bars of 21 memory devices.
Each memory device has a capacity of 16,384 bits so that one memory slave card contains 64K21 bits and the complete module contains 512K21 bits.
The word size of 21 bits is necessary for the normal 16 data bits and 5 error correction bits, in order to have the possibility to detect and correct one error.
The memory cells in the memory device are organised into a matrix of 128 x 128 cells.

The 14 address bits required to decode 1 of the 16,384 cell locations within the memory device are multiplexed onto the 7 address inputs and latched into the on chip address latches by applying two negative going TTL clocks. The first clock, the Row Address Strobe (RASN) latches the 7 row address bits into the chip. The second clock, the Column Address Strobe (CASN) latches the 7 column adddress bits into the chip. These 7 addresses, CASN and the read/write signal WEN are offered to all memory devices on all cards without decoding.

Selection between the different bars of 16K21 memory is done by gating the RAS clock with a CS(Card Select) and RB(Ras Bar). So only one RAS-N clock, and thus one bar of memory devices, is activated at a time.
The input for the clocks RAS and CAS are derived from the Memory Timing circuitry.
Due to the dynamic nature of the memory devices used, each of the 128 rows of the memory device matrix must be refreshed every 2 msec to maintain data.
In order to limit the number of refresh cycles, all memory devices on all memory slave cards are refreshed at the same time.
During Refresh the selection on RAS, Card Select and Ras Bar, are overruled and all RASN clocks are activated, and therefore all memory devices. At the same time the CASN clocks are kept inactive (high) to avoid output bus contention, while the outputs of 4 bars on a card are 'wire ORed'.

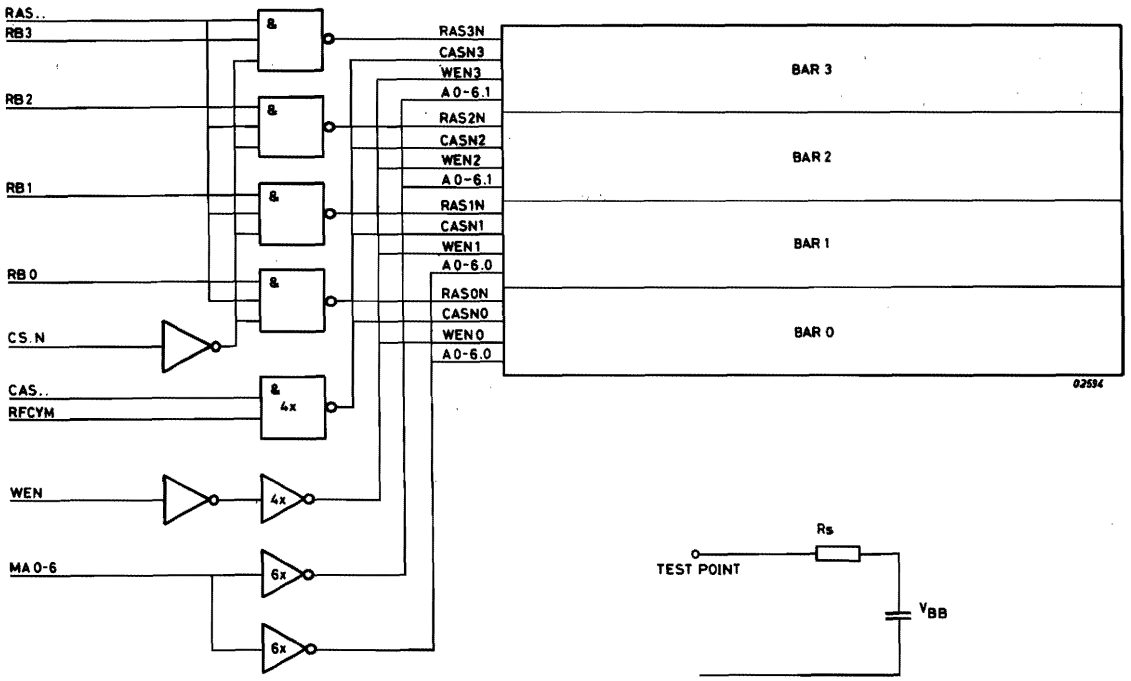


Figure 3.1 MEMORY ARRAY ADDRESSING AND BAR DECODING (1 SLAVE)

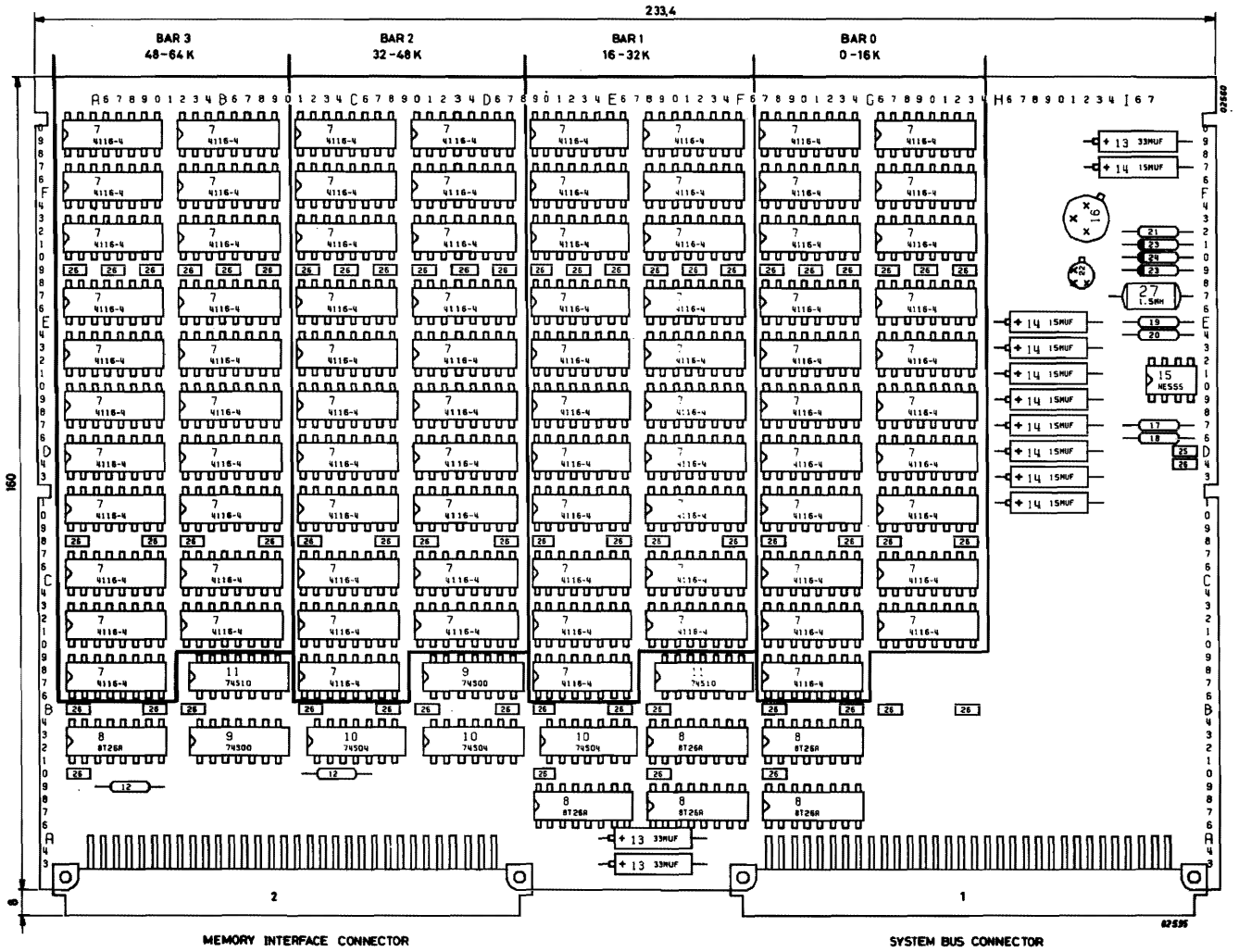


Figure 3.2 PHYSICAL LOCATION OF THE MEMORY ARRAY ON 1 SLAVE

3.3 RAM DESCRIPTION

The RAM used in the memory module uses a device manufactured by Mostek (MK4116P-4). The features are:

a) 16,384 x 1 bit organisation
b) standard 16-pin package
c) standard +12V, +5V, -5V power supplies required
d) low power - 462mW active, 20mW standby
e) all inputs (including clocks) and output TTL compatible
f) 128 refresh cycles every 2 msecs
g) output data controlled by CAS-N and unlatched at the end of the cycle
h) access time 250 nsec, read/write cycle time 410 nsecs

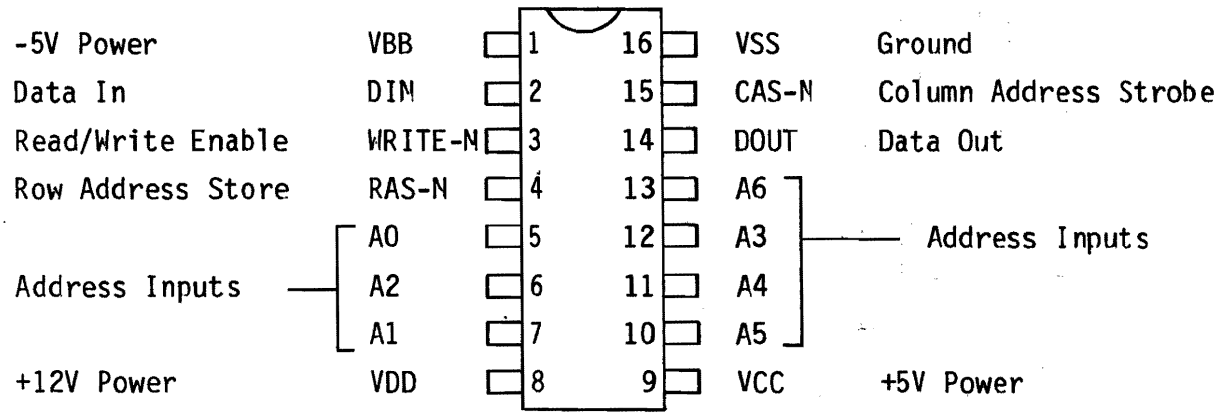


Figure 3.3 RAM PIN CONFIGURATION

The following pages indicate internal chip timing relationships for Read Cycle (figure 3.5). Write Cycle (figure 3.6) and Refresh Cycle (figure 3.7), as well as a simplified Block Diagram of the RAM (figure 3.4).

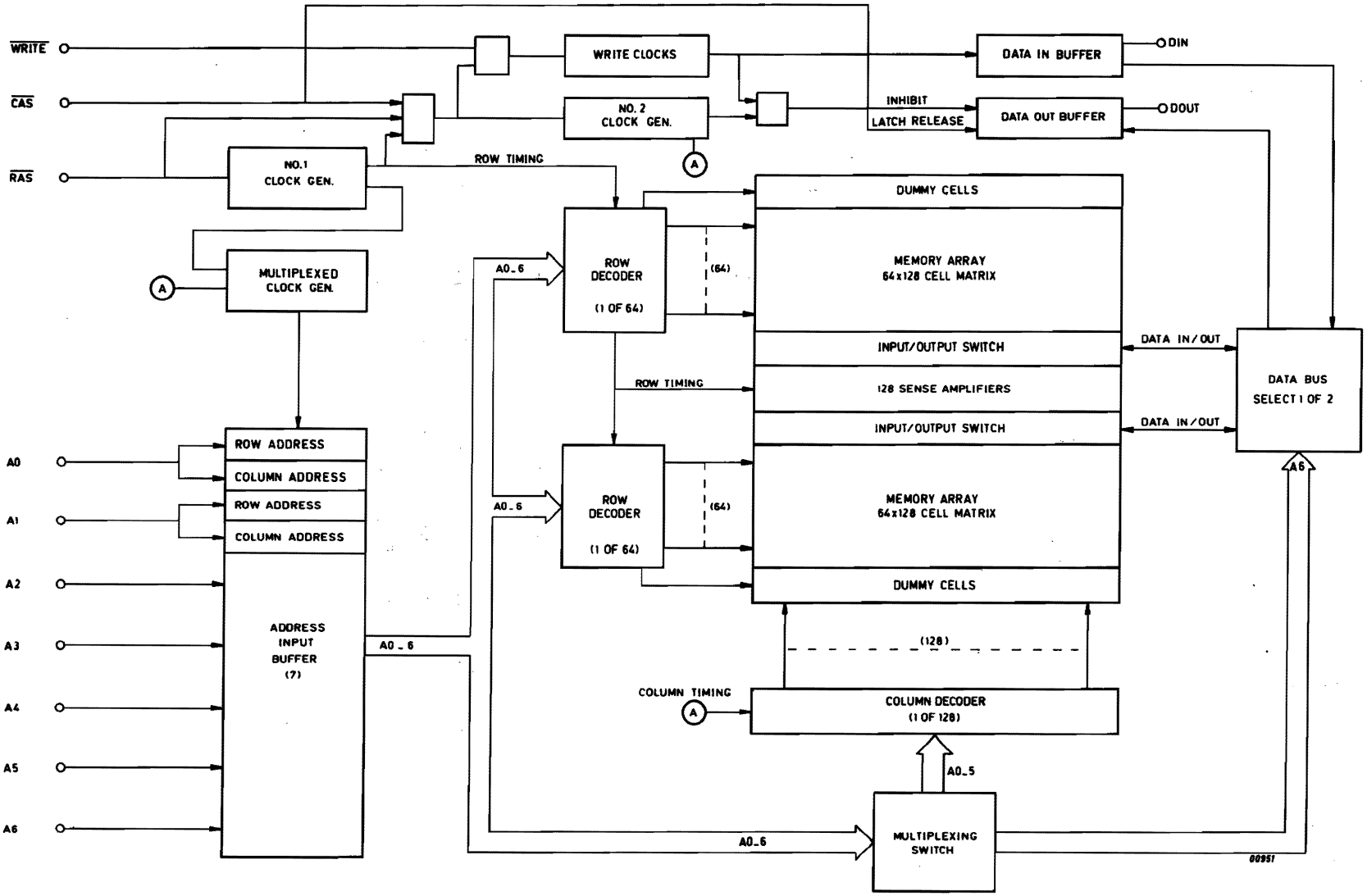


Figure 3.4 RAM BLOCK DIAGRAM

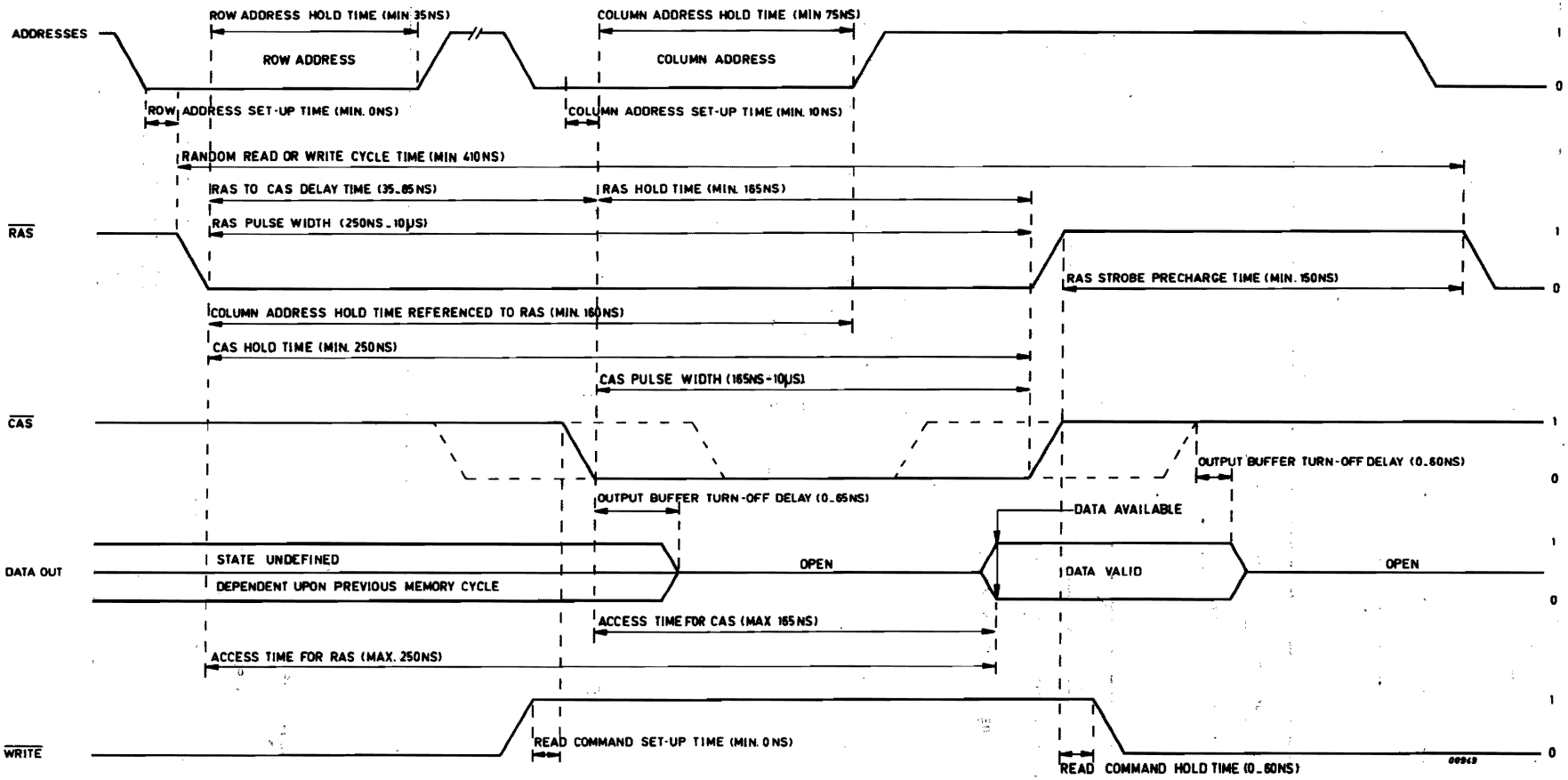


Figure 3.5 READ CYCLE TIMING DIAGRAM

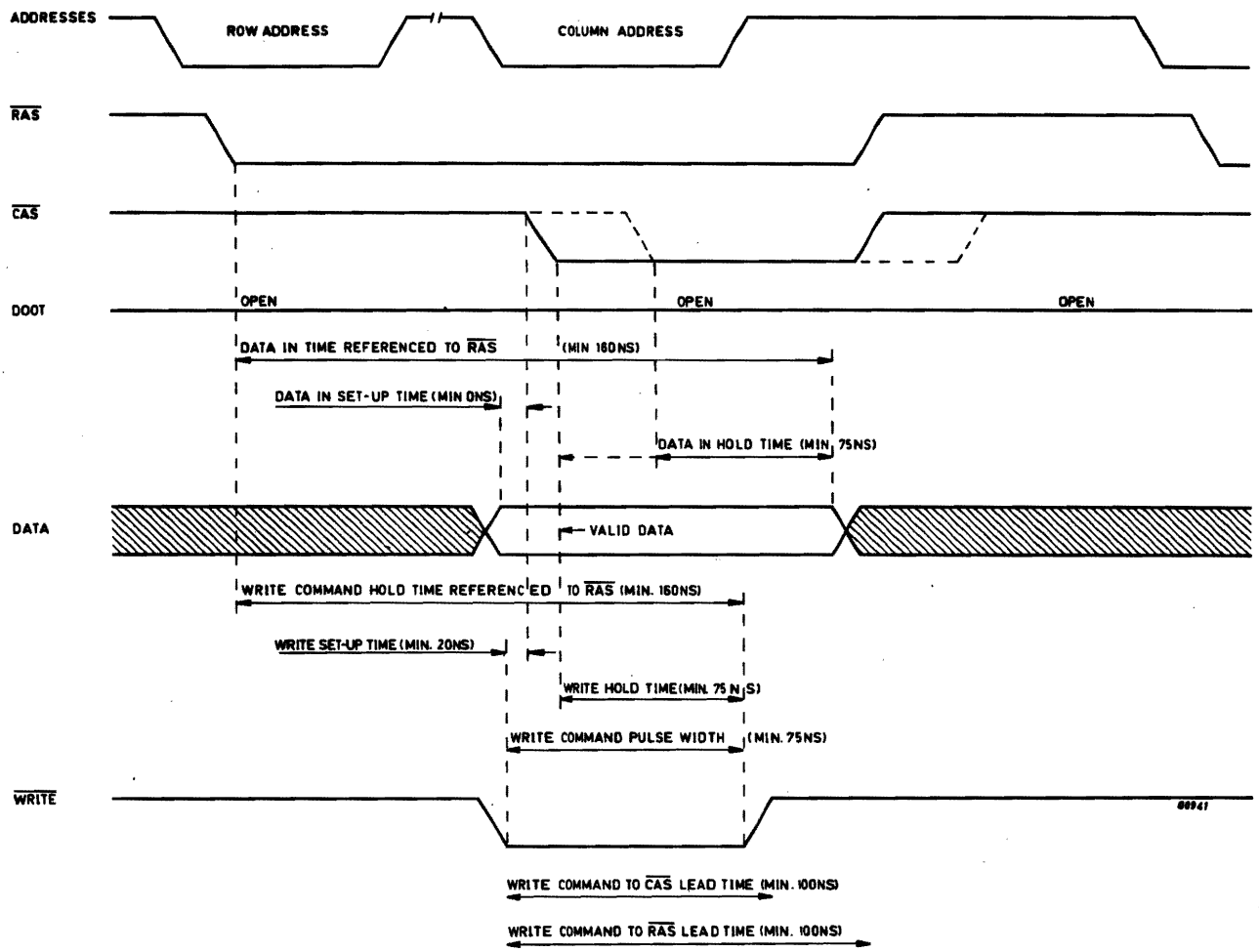


Figure 3.6 WRITE CYCLE TIMING DIAGRAM

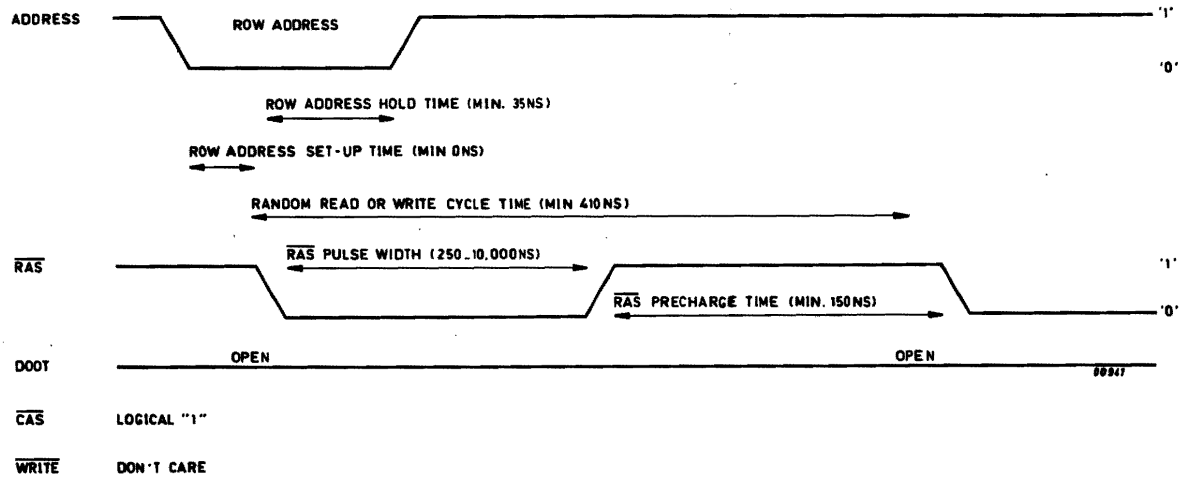
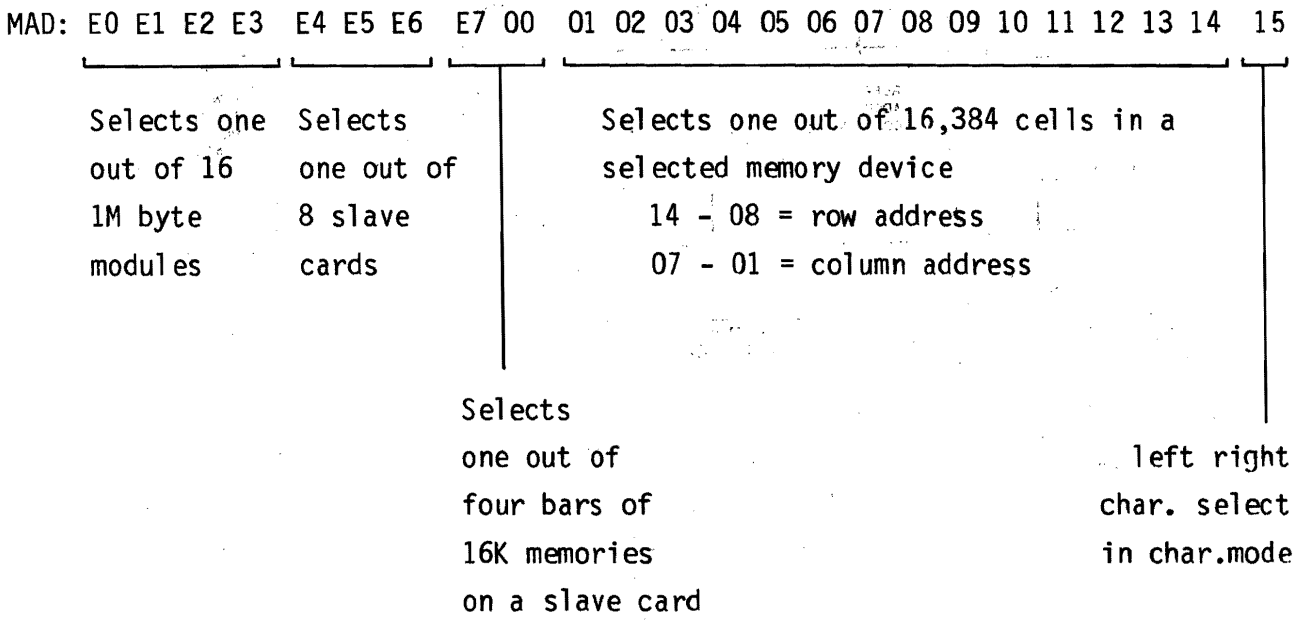


Figure 3.7 REFRESH CYCLE TIMING DIAGRAM

3.4 ADDRESS SELECTION (See figure 3.8)

3.4.1 GENERAL

There is a total of 24 address bits used for the address selection, organised as follows:



Due to the requirements to switch off the address on the UPL bus after ACN it is necessary to store all addresses at the begin of the memory request until the end of the internal memory cycle. Therefore all the addresses are latched, the latch signal LDABN (Latch Data Address Buffer) is derived by ORing TMR) Memory Request) and CYBUSY (Cycle Busy).

For examples of module select and card installation, see chapter 1.6

3.4.2 MEMORY DEVICE ADDRESSES

The memory devices need to be addressed twice within a cycle in order to select a cell. So the memory device addresses (MAD01-14) are multiplexed, and selected by timing signal MX.L/R.

The addresses are output in parallel for the left and right hand memory cards for timing and fanout reasons. On each memory slave card the addresses are buffered again with two buffers. So each buffer has a load (only capacitive) of 42 memory devices.

At the start of a cycle MXL/R is low and the MAL14-08 lines are choosen and offered as A0-A6 to the memory devices, they are latched into the memory device with the RAS clock.

When the row addresses are latched in, the MXL/R signal becomes high and the MAD07-01 lines are choosen and offered, as A0-A6 again to the memory devices but latched in now by CAS (Column Address Strobe).

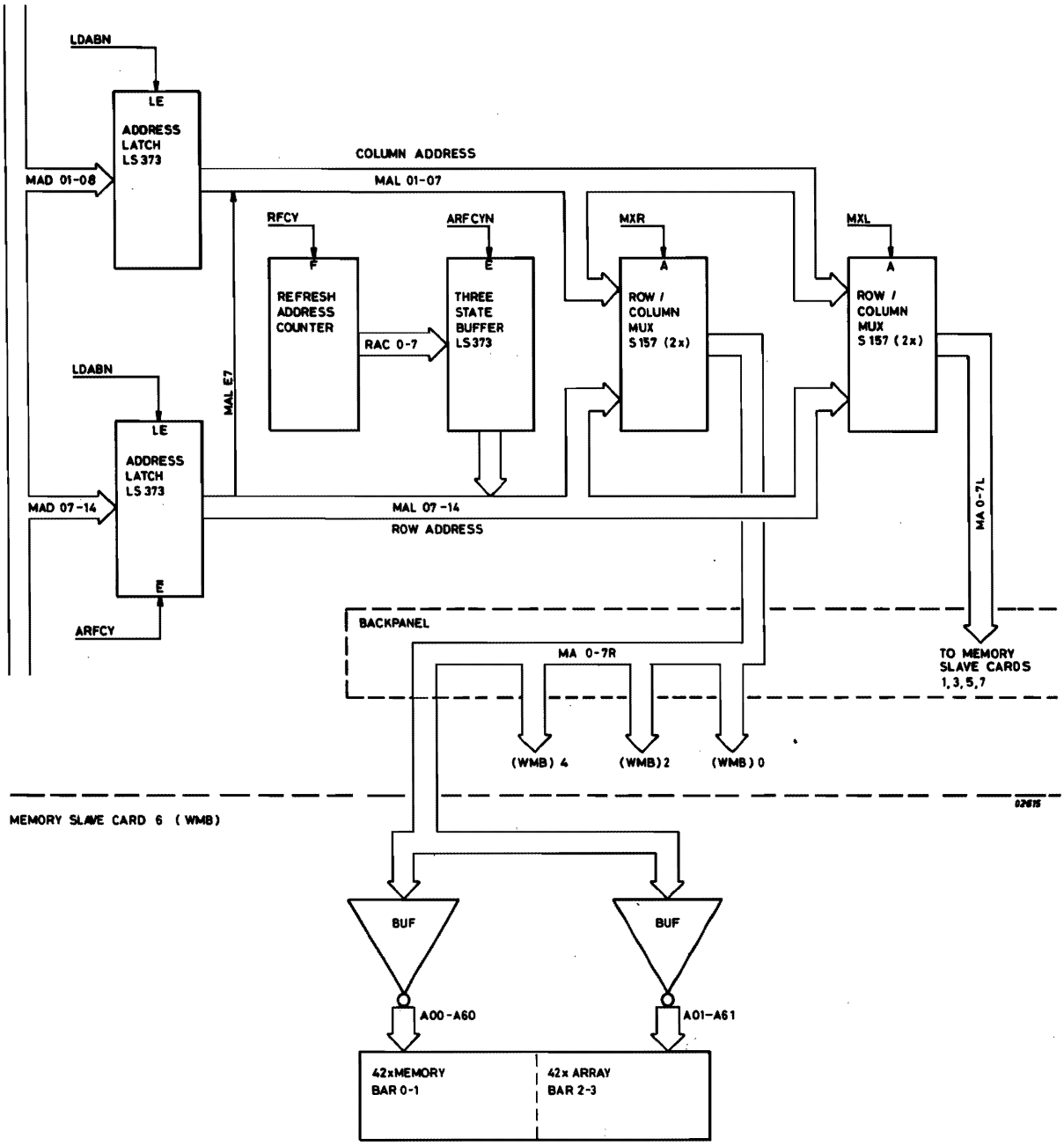


Figure 3.8 MEMORY DEVICE ADDRESSING

During a refresh cycle the output of the address input latch for MAD14-08 is disabled and the output of the refresh address counter buffer is enabled. The refresh addresses are now buffered as the Row addresses to the memory array.
In case of battery stand by mode the refresh address, must still be offered to the memory devices so only the latch for the column addresses can be switched off.

Future 64K memory addressing
The somewhat confusing wiring of MAL07 is made for possible future use of this control card with 64K memory devices. Therefore MAL07 is wired as the least significant column address for 16K memory devices and also as the most significant row address for 64K memory devices.

3.4.3 BAR SELECTION (See figure 3.9)

The MAD00 and MADE7 address bits are used for the selection of one out of four bars of memory devices on a slave card. The address bits are decoded on the control card to provide the signals BAR0-3. These four selection lines are buffered and 'ANDED' with RFCYNB (Refresh Cycle Not Battery).
The buffered signals RB0-3 (Ras Bar) are offered over the backpanel to all slave cards to select one RAS clock per card. So each RB signal has a load of eight gates. In normal Read, Write cycles RFCYNB is high but in a Refresh cycle RFCYNB is low and all RB lines are high, now all RAS buffers are activated. During Battery Stand By mode only the RB buffer and the RAS buffers are kept active and the address latch for MAD00. MADE7 and the decoder are switched off.

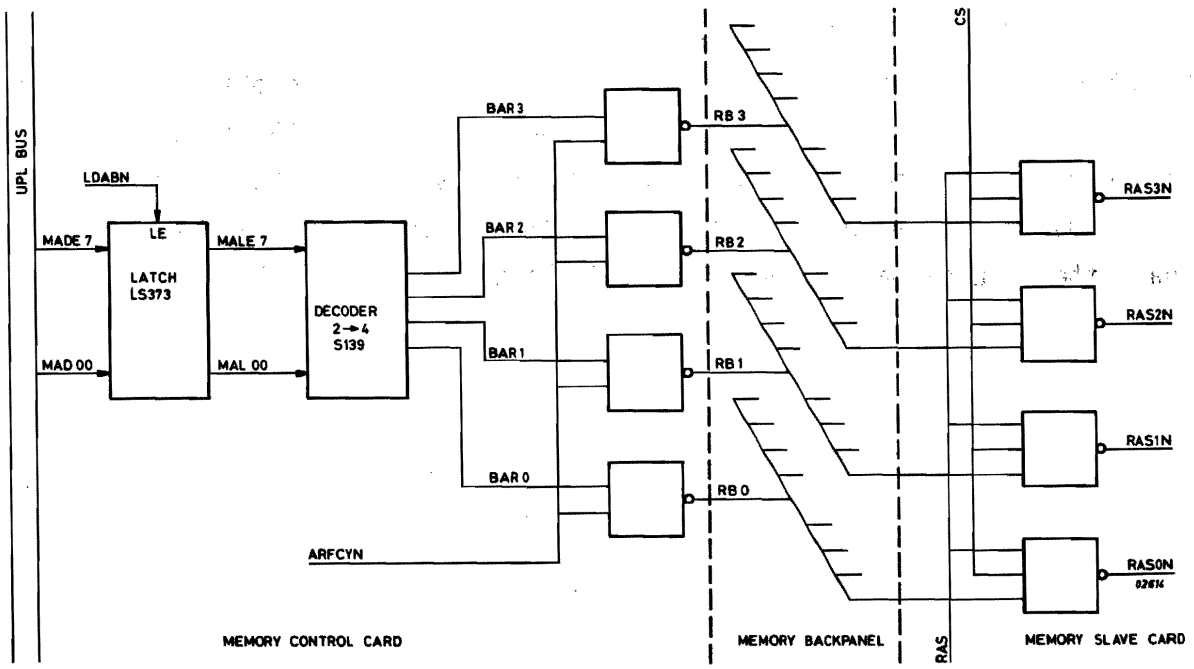


Figure 3.9 BAR SELECTION

3.4.4 CARD SELECT AND MEMORY PRESENT (See figure 3.10)

The MADE6, MADE5 and MADE4 address bits are used for the selection of one out of eight memory slave cards. The address bits are offered to a decoder which has as output eight select lines SO-7N. These signals are 'and' with RFCYN (Refresh Cycle Not). The now obtained signals CSO-7N (Card Select Not) are offered each to one memory slave card.
Only the memory slave card which receives a CS-N signal (low is active) is enabled, and can generate a RAS-N signal to the memory devices, also only the selected card can put data on the MIOB lines during a READ cycle (in conjunction with EMDO).

CS-N is a low active signal in order to prevent excessive power current (P12P) in the memory when power is switched on without a memory control card.
In a Refresh cycle RFCYN is low and all CS-N outputs will be low too now all memory slave cards are activated simultanously.

The address bits MADE6-E4 are also given, after latching, to a demultiplexer to select one out of eight MPR-N signals (Memory Present Not).
If the selected MPR-N signal is high it means that no memory slave card is present on the requested card location and the signal CS (Card Select) will be low. Now it is not possible to start a Read/Write cycle and to select that memory slave card location. On the other hand when the requested card is present MPR-N is low, now CSEL will become high and both timing and card select are enabled.

3.4.5 MODULE SELECT (see figure 3.11)

The MADE0-E3 address bits are used for the selection of one complete 1M byte module out of 16 possible modules (Total address feed is 16M byte).
The latched addresses are compared with four signals ACE0-3 (Address Compare Extension) which can be strapped. When the contents of the two four bits is equal, the MSEL signal becomes high and the module is selected.

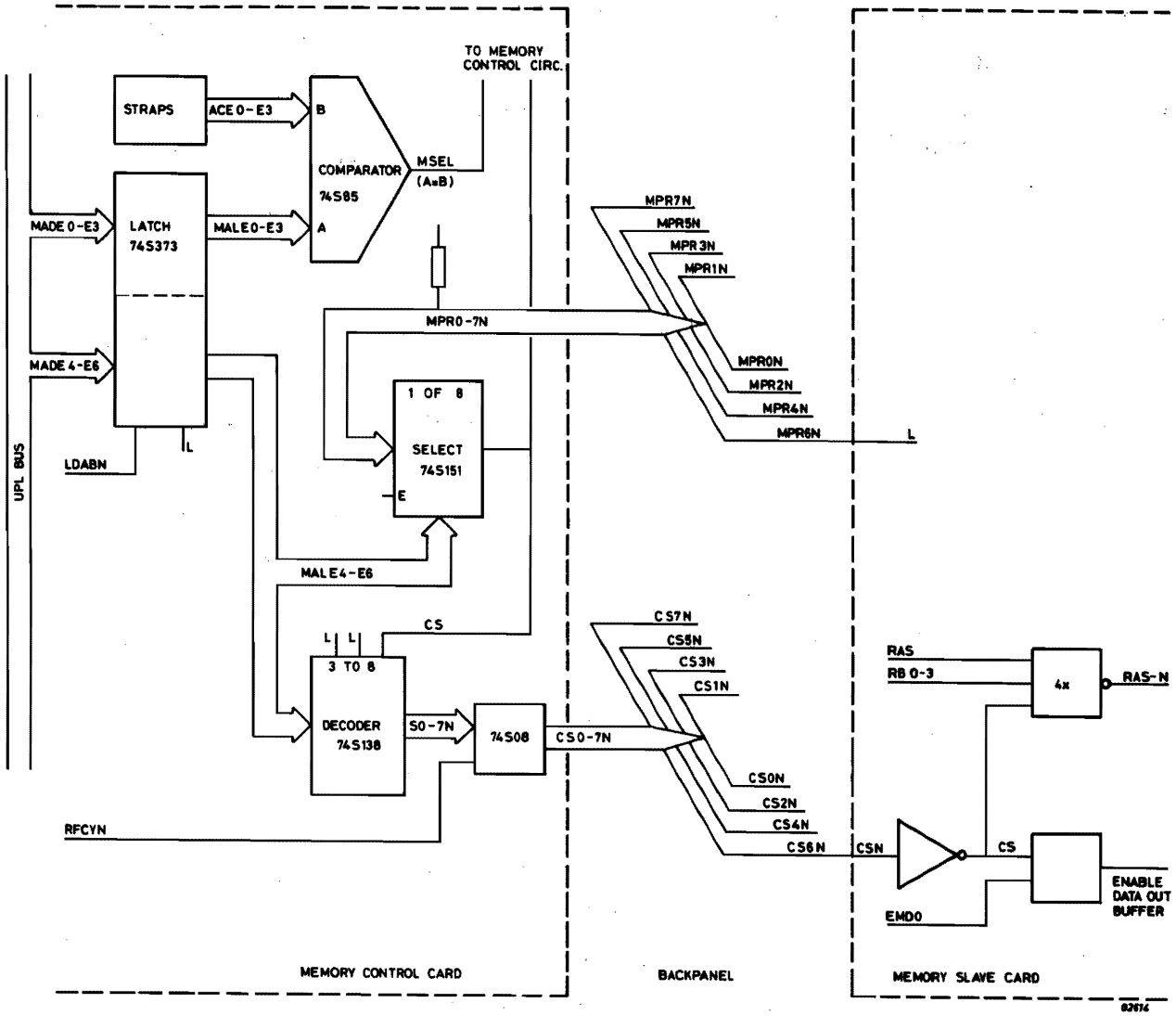


Figure 3.10 CARD SELECTION AND MEMORY PRESENT LOGIC

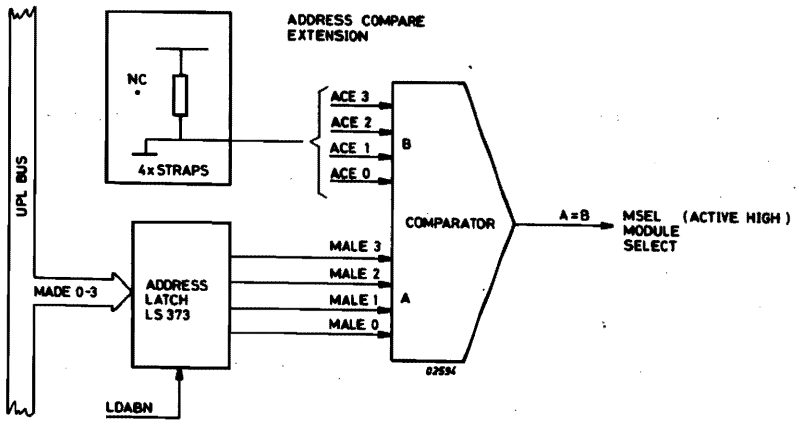


Figure 3.11 MODULE SELECTION LOGIC

3.4.6 REFRESH ADDRESSING

A mention will also be made here to the Refresh Address Counter which provides a 7-bit row address during a refresh cycle (see Timing Refresh Cycle). It consists of two 4-bit counters in cascade - that is effectively an 8-bit counter counting to 256 (actually 0 to 255). During refresh, we must select one of the 128 rows in each RAM so the MSB of this counter is not used and it effectively counts from 0-127.

The counter is never cleared (because LT2 and LT3 are continuously low since the initial state of the counter is totally irrelevant) and is clocked by the signal RFCY, indicating that a refresh cycle is taking place. As the counters clock on the H→L clock transition, the Refresh Address Counter increments by one at the end of each refresh. The outputs of the counter, RAC(0-6), are offered via a three state buffer to the row inputs of the address multiplexer.

3.5 DATA TRANSFER LOGIC

3.5.1 GENERAL

As mentioned previously, there are six different forms of memory cycle - Read and Write of Word/Left character /Right character.
The following diagrams illustrate a simplified data flow for each of the six cycles described in the following text. Table 3.1 displays the various control signals necessary for each of these cycles.
Data is inverted twice in the memory module, once at the BIO-N transceiver so all data on the control card and so also the data on memory interconnect backpanel is inverse and opposite to data on the UPL bus. Data is inverted a second time between the internal memory bus and memory array. So data stored in the memory array has the same polarity as data offered on the UPL BUS.

3.5.2 WRITE WORD CYCLE (See figure 3.12)

Data to be stored is present on the UPL bus as BIOOO-15N. In the word mode, transceivers 1 and 3 have open receivers and data is offered through latches 1 and 2 to the memory slave cards as MIOBOO-15.
Data is latched into latches 1 and 2 at the start of the internal memory cycle in order to have the possibility to release the UPL bus.
The MIOBOO-15 signals are also directed, through the transparant data out latches 3 and 4 to the parity circuitry.
During a write cycle the check bit inputs of the parity circuitry are made low (MDOLSO-S4) and the parity circuitry will generate the five required check bits SEVO-4.

These check bits are offered, through the driver of transceiver 4, to the memory slave cards as MIOBS0-S4.

Data to be stored and checkbits are buffered again on each slave card by the receivers of transceivers 5, 6 and 7. This buffered output MDI00-15. S0-S4 is given to the memory devices on all cards. This data will only be written on the selected bar of memory devices by means of WEN.

Signal[1]	Inverted Signal	READ WORD	WRITE WORD	READ LEFT CHAR	READ RIGHT CHAR	WRITE LEFT CHARACTER 'READ'	WRITE LEFT CHARACTER 'WRITE'	WRITE RIGHT CHARACTER READ	WRITE RIGHT CHARACTER WRITE
WRITE(V)	READ	L	H	L	L	H	H	H	H
CHA(V)	CHAN	L	L	H	H	H	H	H	H
MAD15	AD15N	*	*	L	H	L	L	H	H
RENCY		L	L	L	L	H	H	H	H
RDCY	RDCYN	L	L	L	L	H	L	H	L
RCY		H	L	H	H	L	L	L	L
WCY	WCYN	L	H	L	L	L	H	L	H
ELCH	ELCHN	H	H	H	L	H	H	L	L
ERCH	ERCHN	H	H	L	H	L	L	H	H
EDIBLN		H	L	H	H	H	L	H	H
EDIBRN		H	L	H	H	H	H	H	L
EDOBLN		H	H	H	H	H	H	H	L
EDOBRN		H	H	H	H	H	L	H	H
TRDO		H	L	H	H	L	L	L	L
TRDOL		H	L	L	L	L	L	L	L
TRDOR		H	L	L	H	L	L	L	L
TRDOLR		L	L	H	L	L	L	L	L
LDABN		[2]							
LDOBN(at time T5)		L	L	L	L	H	L	H	L
LMDO		[3]							
EMDO		H	L	H	H	H	L	H	L
SF		[4]	*	[4]	[4]	*	*	*	*
ENERCH		[5]	L	[5]	[5]	L	L	L	L

*) don't care or not determined
1) logic direction of the signal is given for the true signal
2) high during the internal cycle for latching Data in
3) signal is equal in all kind of cycles, low during Ras id high (LMDO : low = latch transparant, high = high = latched)
4) SF = L in case of no error, H in case of error
5) ENERCH = H in case of detected error, low case of error

Table 3.1 DATA TRANSFER SIGNALS

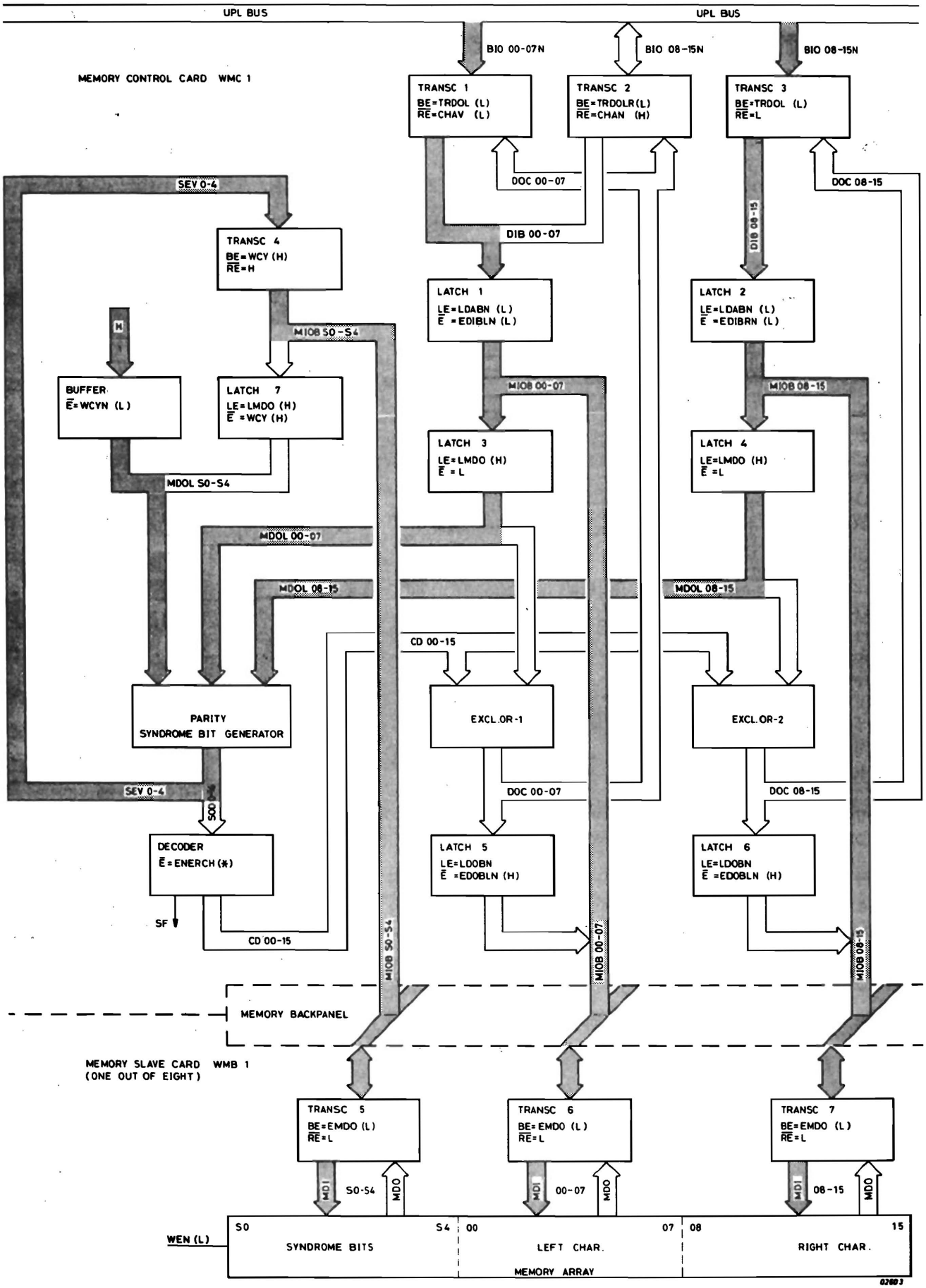


Figure 3.12 WRITE WORD CYCLE

3.5.3 READ WORD CYCLE (See figure 3.13)

Data is read out of the memory array as MDOOO-15 and checkbits MDOSO-S4. Only the selected memory slave card is enabled to drive data (MIOBOO-15, SO-S4) through transceivers 5, 6 and 7, via the memory backpanel to the control card. The data bits (MIOBOO-15) are offered directly through the transparant data out latchws 3 and 4, the switched off correction circuits (exclusive or's) and the Bus drives (part of transceivers 1 and 3) to the UPL bus (BIOOO-15N) as being not corrected data.

All data and check bits, (MDOLOO-15, SO-S4), are given to the parity circuitry which will generate the 5 syndrome bits SEVO-4 (Sigma Even) and their complements SODO-4 (Signal Odd). If no error is indicated by these S-bits (SF=L) the outputs of the error decoder are kept low and the data offered to the UPL bus remains unchanged.

If there is an error (SF = H) the error decoder is enabled and the failing data bit can be corrected. Data on the UPL Bus will be valid later on in the cycle. At the end of the internal Read cycle the data out is latched, into latches 3, 4 and 7 until the next Read or Write cycle.

3.5.4 READ LEFT CHARACTER (See figure 3.14)

This cycle is very nearly identical to the Read word cycle except that in the character mode the right character driver (Trans-1) BIOOO-07N is disabled, this will be guaranteed for the complete cycle.

The data of the right hand character (octad) is now driven by Trans-2 to the UPL-BUS as BIOO8-15N, while the driver of the left hand character (Trans-3) is disabled.

3.5.5. READ RIGHT CHARACTER (See figure 3.15)

This is similar to Read Left character, except that now the Right hand character of memory is enabled to put data on the right hand character of the UPL-BUS. Drivers of transceivers 1 and 2 disabled and of Trans-3 enabled.

3.5.6 WRITE LEFT CHARACTER (See figure 3.16)

The Write Left Character cycles are rather more complicated, requiring as they do part of the memory word being retained and rewritten together with the new character. This requires two sucessive memory cycles, the first to read a word from the desired address and, if necessary, correct it, and the second to select the desired "new" character and the supplement "old" character and write them back into the same location as a word.

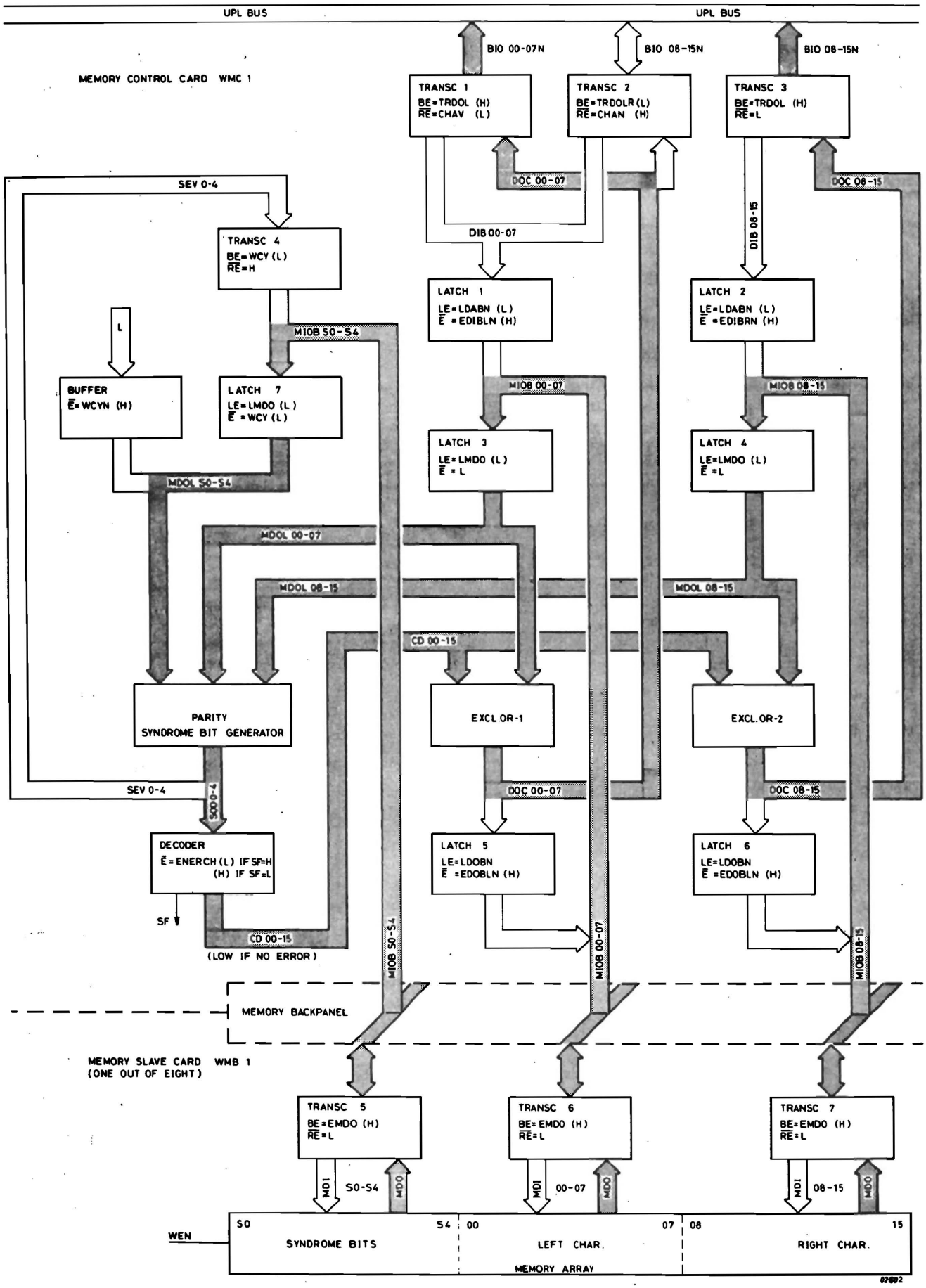


Figure 3.13 READ WORD CYCLE

The 'read' part looks like a normal read cycle with the following differences:

- The UPL-bus drivers, of transceivers 1, 2 and 3 are disabled. So no data out is put on the BIO-N lines.
- The errror correction decoder is always enabled to speed up correction in case of error.
- The corrected data DOC00-15 is latched into latches 5 and 6 at the end of this 'read' cycle.

Also the write part is very similar to a normal word cycle however data to be written is now derived from two different sources.

- The new character (BI008-15N) is gated through BUS receiver (of transceiver 2) and latch 1 to the MIOB00-07 lines (receiver of trans 1 and latch 2 being disabled).
- The complement old character is offered by latch-6 to the MIOB08-15 lines (latch 5 stays disabled).

So now a complete word is available which can be handled as data in a normal write cycle.

3.5.7 WRITE RIGHT CHARACTER (See figure 3.17)

This cycle is nearly identical to the write left character cycle, with the exception that the new data for the Right character is gated via latch 2 while latch 1 is disabled.

The complement old character is released by latch 5 while latch 6 is disabled.

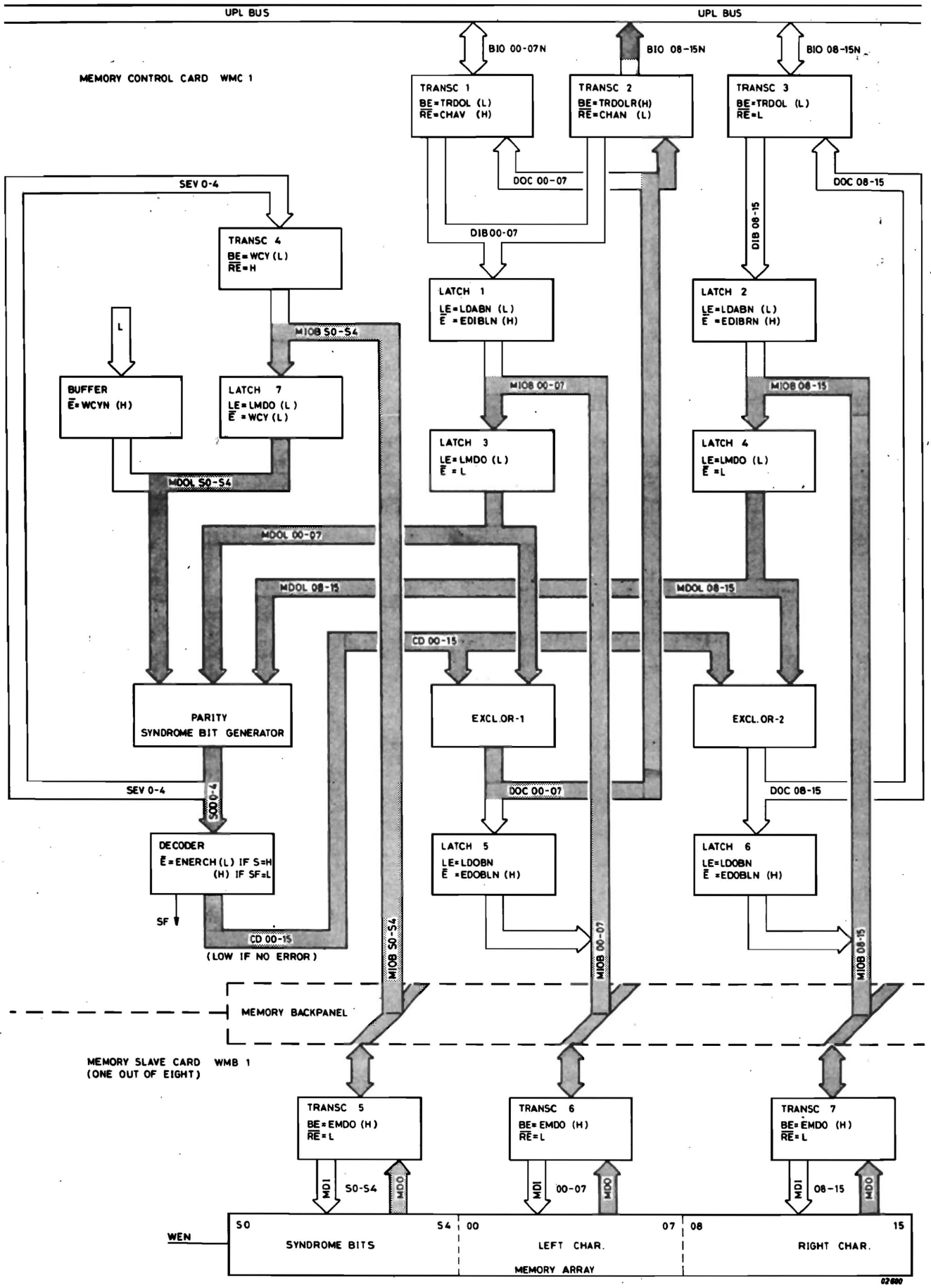


Figure 3.14 READ LEFT CHARACTER

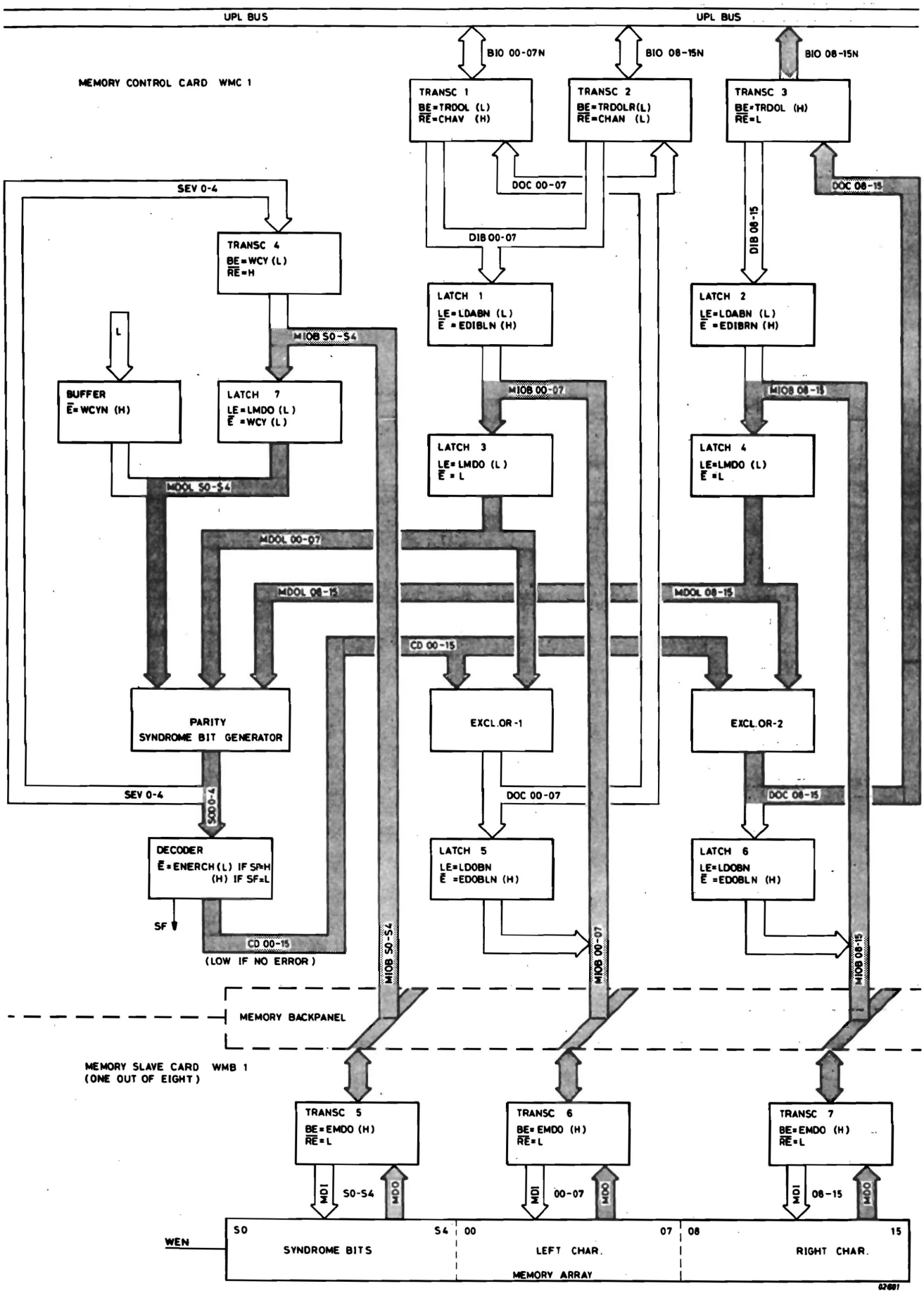


Figure 3.15 READ RIGHT CHARACTER

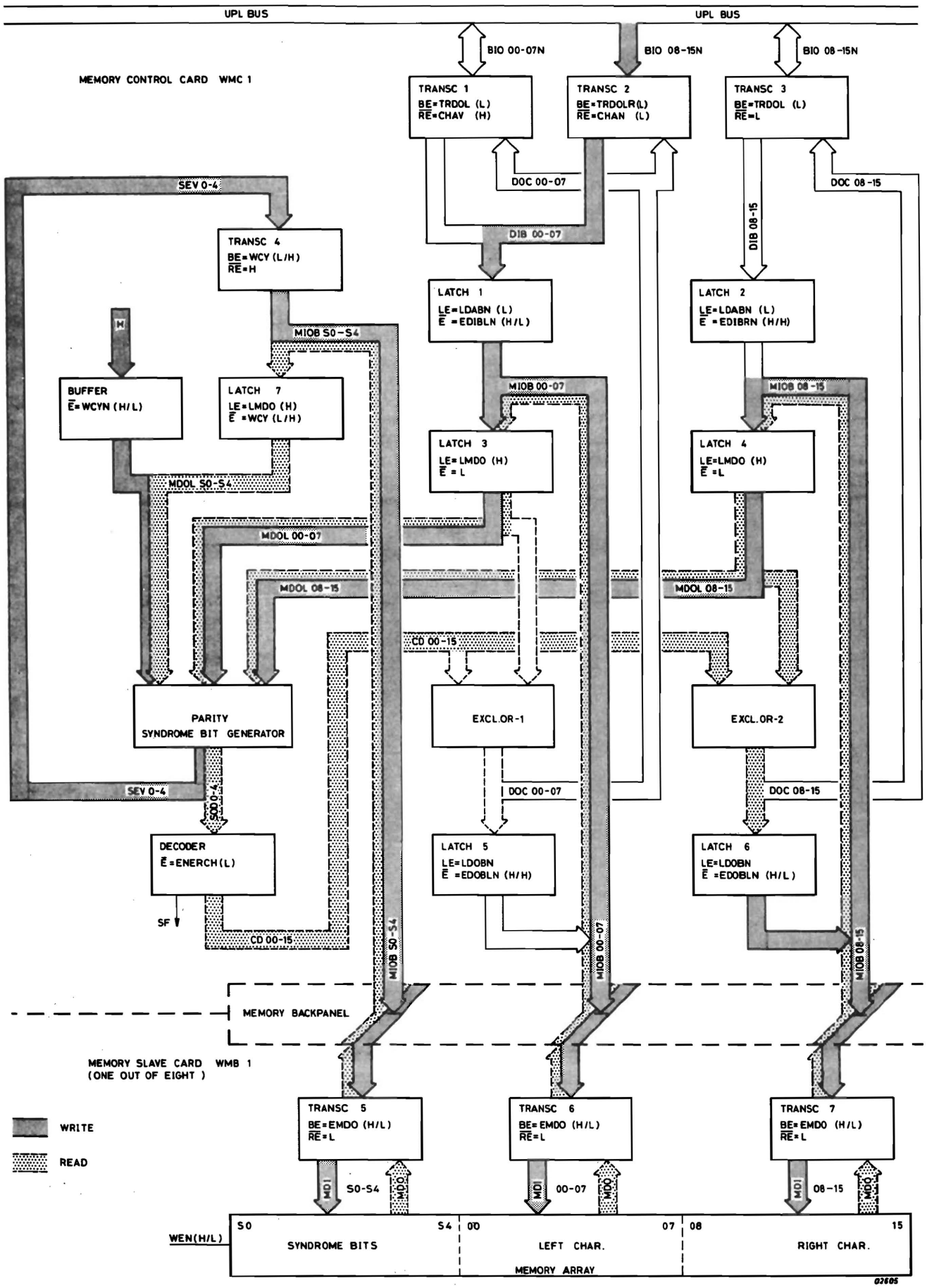


Figure 3.16 WRITE LEFT CHARACTER

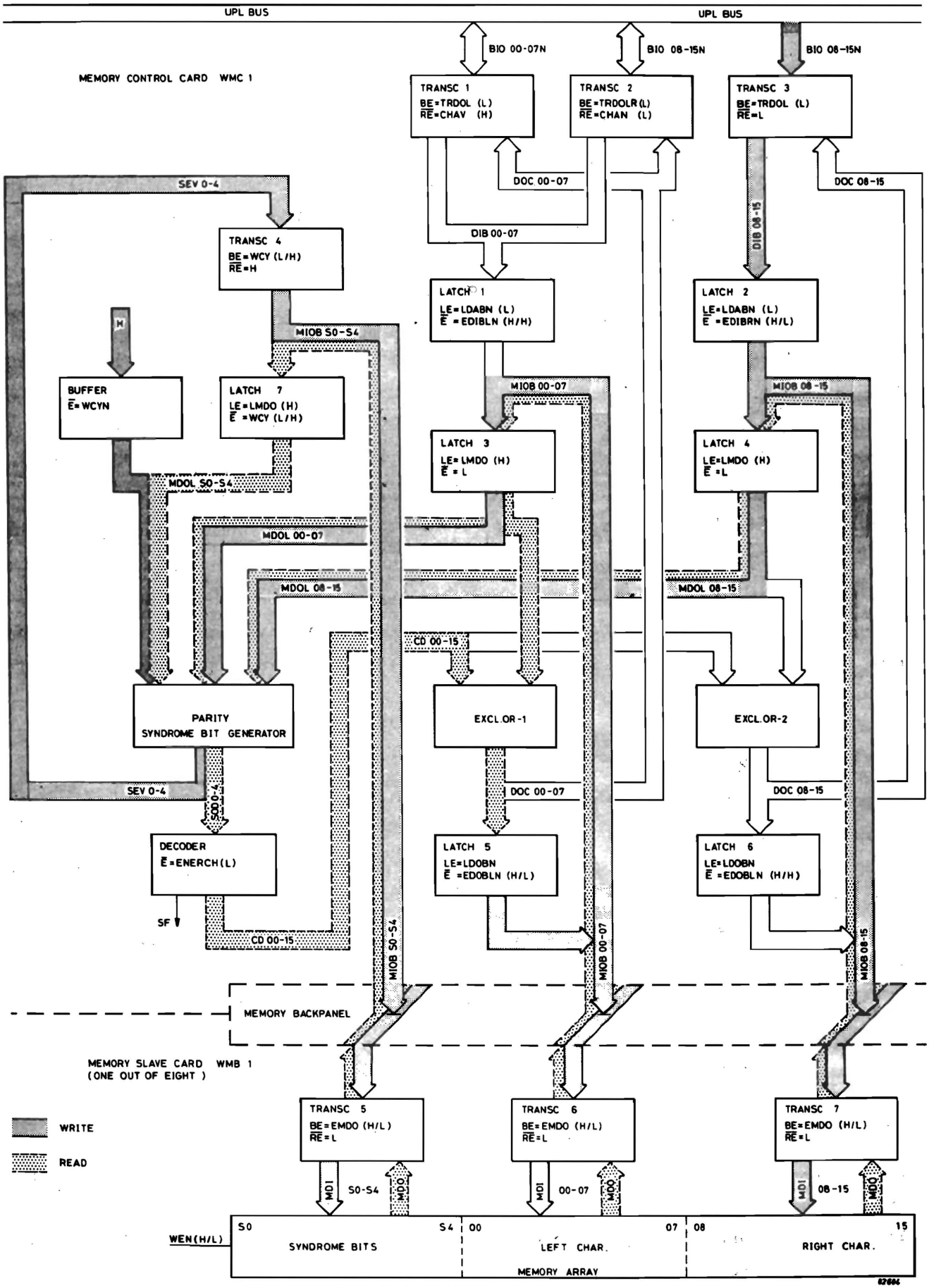


Figure 3.17 WRITE RIGHT CHARACTER

3.6 DATA I/O LOGIC (see figures 3.12-3.17 and figure 4.4)

The data I/O logic can be sub divided into 6 main areas:

3.6.1 - UPL Interface, Transceivers 1, 2 and 3

3.6.2 - Data In Latches 1 and 2

3.6.3 - The Memory Data Out Latches 3 and 4

3.6.4 - The Error Correction Exclusive OR's

3.6.5 - The Write Character Intermediate Latches 5 and 6

3.6.6 - The Memory Array Transceivers

3.6.1 UPL INTERFACE, TRANSCEIVERS 1, 2 AND 3

All interfaces between the UPL-BUS, BIO-N lines and the memory module are through the transceivers 1, 2 and 3 (in total 6 devices 8T26A).

In word mode, the transceivers 1 and 3 are used. For read, the outputs are enabled by TRDOL and TADOR as long as TMRN is low. In a write cycle, all bus drivers are switched off and the transceiver acts as a receiver for Data In.

Transceiver 2 fulfills a multiplex function for data I/O between the right hand UPL character (BIO08-15N) and the left hand character of memory (DIB00-07). This means that the control card presents a double load on the BIO00-08 lines. Although this is normally not allowed, dispensation has been given for this design because there is at least one memory slave card which is not connected to the UPL bus.

3.6.2 DATA IN LATCHES 1 AND 2

Data In is latched into latch 1 and 2 (74LS373) by LDABN for the complete internal cycle.

In a write word cycle, both latches are enabled by EDIBL/RN being low (Enable Data In Left/R Not), and data (MIOB00-15) is offered to the memory slave cards and the parity circuits (74S280). In a write character cycle, only that latch is enabled which has to drive the new data character to the memory array, so in Write Left character latch 1 is enabled (EDIBLN=L), and latch 2 disabled (EDIBRN=H).

During Read cycles both latches 1 and 2 are disabled.

3.6.3 MEMORY DATA OUT LATCHES 3 AND 4

The memory data out latches 3 and 4 (74LS373) are used both in read and write cycles.

At the beginning of a read cycle the latches are transparent, this means that Data Out can pass through them directly.

At the end of the read cycle, Data Out is stored until the beginning of a new read or write cycle.

In a write cycle, use is also made of the transparant period of the latch to drive the data to the parity circuitry.
The output of these latches are always enabled.

3.6.4 CORRECTION CIRCUIT, EXCLUSIVE OR'S

The exclusive or's are part of the error correction circuitry although data out is always allowed through as part of the data out path. In a 'NO ERROR' state, all CDOO-15 (correction data) signals will be low, and data before and after the circuits is identical. If there is a single bit error, one of the CD-lines becomes high and the corresponding data out bit is inverted and thus corrected.

3.6.5 WRITE CHARACTER INTERMEDIATE LATCHES 5 AND 6

The latches 5 and 6 serve as an intermediate latch to store the data read out in the read part of a write character cycle. The data out is only latched into this latch at the read part of a Write character cycle.
Only the latch opposite to the new character to be written in is enabled (by EDOBL/RN; Enable Data Out Bus Left/Right Not), e.g. in write left character, the right character is enabled by EDOBRN.

3.6.6. MEMORY ARRAY TRANSCEIVERS

On each memory card a number of transceivers (8T26) are placed.
In a write cycle they provide all memory cells with data to be written in. During a read cycle only the selected card will have enabled bus drivers (EMDO; Enable Memory Data Out) to put the data read from the memory device on the internal data bus (MIOBOO-15).

3.7 ERROR CORRECTION CIRCUITRY

The error correction-circuity for this memory is made by means of standard MSI and SSI schottky TTL's in order to obtain a faster memory (both access and cycle time) than is possible with the Error Correction LSI used on the WMA memory card. However, the same check bit generation and card error detection scheme is used in order to have similar test patterns for testing the error correction function on both designs.
For minimizing the number of TTL's in the error correction, the same parity circuits (5x 74S280) are used for Check bit generation in a write cycle and for Syndrome bit generation in a read cycle.

3.7.1 CHECK BIT GENERATION IN A WRITE CYCLE

Check bit generation is made by Exclusive OR-ing, that means performing a parity check, on different groups of data bits, in accordance with a "modified" Hamming code. For check bit generation all not used inputs, so also the check bit inputs used in read cycle, must be low. This is achieved by disabling the data out latch for check bits (MDOLSO-4) by WCY and enabling Buffer 1 (74LS240) by WCYN='L'. The check bit inputs are put in the low state. The check bits are generated by the following logic equatation.

SOD 0 = MDOL 00 ⊕ 01 ⊕ 02 ⊕ 03 ⊕ 04 ⊕ 05 ⊕ 06 ⊕ 07
1 = MDOL 00 ⊕ 01 ⊕ 02 ⊕ 06 ⊕ 10 ⊕ 11 ⊕ 13 ⊕ 15
2 = MDOL 00 ⊕ 03 ⊕ 09 ⊕ 11 ⊕ 12 ⊕ 13 ⊕ 14 ⊕ 15
3 = MDOL 01 ⊕ 03 ⊕ 04 ⊕ 05 ⊕ 08 ⊕ 12 ⊕ 13 ⊕ 14
4 = MDOL 02 ⊕ 04 ⊕ 07 ⊕ 08 ⊕ 09 ⊕ 10 ⊕ 14 ⊕ 15

SOD = Sigma Odd

Note that MIOBSi and SODi have the same direction by being SEV (Sigma Even) the complement of SOD and the memory slave card Bus driver (Transceiver-7, 8T26A) is also inverting.
Check bits and data bits are written into the memory array at the same time on the same address.

3.7.2 ERROR DETECTION-CORRECTION DURING A READ CYCLE

The data bits and check bits (MDOL00-15 and SO-S4) read from the memory array are offered to the parity circuits, (Latch-7 is enabled and buffer 1 is disabled).
The parity device will now generate a new check bit which is derived from the data bits. This new check bit is compared with the 'OLD CHECK bit' formed during the previous write cycle.

The output of this comparison is called Syndrome bit, and it is generated by the same parity device used in the previous write cycle for generating the old check bit.
In a NO ERROR state, the old and new check bits are equal, the output syndromebits SODO-4 are all low, and the SEVO-4 all 'high'. These latter outputs are used in a separate decoder (5 input NAND gate 74S30) to indicate to the timing circuitry that there is no failing data bit ((There is a separate decoder for no error (SF = Single Fail), and for error bit indication)).

To prevent decoding glitches in the valid data, which is already driven on the UPL bus, the error bit decoder outputs are disabled by ENERCN going high until SF is valid. If SF indicates no error by being low, the decoder stays disabled and the data out will be equivalent to the data read in the memory.
In case of an error, one or more of the old and new check bits are unequal and the corresponding syndrome bit will become high.
The binary value of the syndrome bits indicate which data or error correction bits fail. SF will now be high indicating an error, and the error decoder is enabled by ENERCN being low.
Decoding of the syndrome bits is done by some combinational logic (74S138, 74S139 and 74S02) to select the data bit which fails.
The Data of the failing bit is simply inverted by means of an exclusive or (74S86) present in the data out path.
So a read cycle with correction takes some additional time and therefore the complete cycle is stretched (access and cycle time).

MDPL	:	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SOD0	=	X	X	X	X	X	X	X	X								
SOD1	=	X	X	X				X				X	X		X		X
SOD2	=	X			X						X		X	X	X	X	X
SOD3	=		X		X	X				X				X	X	X	
SOD4	=			X		X			X	X	X	X				X	X

Table 3.2 CHECK BIT GENERATION

BINARY BIT	:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DATA-CHECK BIT	:		S0	S1	06	S2		11	0	S3	05		01	12	03	13		S4	07	10	02	09		15		08	04			14			
	0		X		X				X		X		X		X				X		X						X						
	1			X	X			X	X		X		X			X				X	X			X									
SIGMA	2					X		X	X					X	X	X						X		X						X			
	3									X	X		X	X	X	X										X	X			X			
	4																	X	X	X	X	X				X	X			X			

Table 3.3 DATA AND CHECK BIT POSITION IN THE ENCODED WORD (MODIFIED HAMMING CHART)

Syndrome bit code											
		SOD2		0	0	0	0	1	1	1	1
		SOD3		0	0	1	1	0	0	1	1
		SOD4		0	1	0	1	0	1	0	1
SOD 1	- 0	C	10	11	12	13	14	15	16	17	← output of 74S138
0	0	0	NE	S4	S3	08	S2	09	12	14	
0	1	1	S1	10			11	15	13		
1	0	2	S0	07	05	04			03		
1	1	3	06	02	01		00				

↑ output of S139

Bit in error, only data bits errors are corrected

NE = No Error

Table 3.4 SYNDROME BIT DECODING

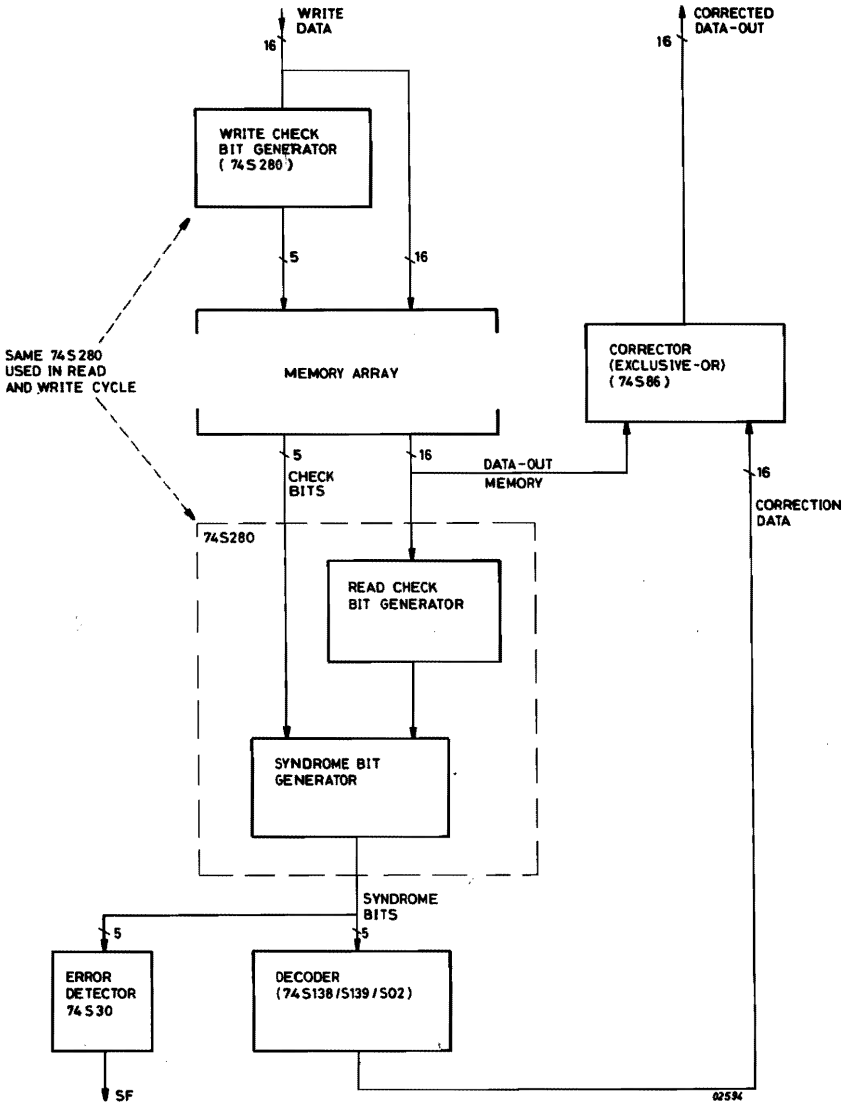


Figure 3.18 BLOCK DIAGRAM OF ERROR CORRECTION CIRCUITRY

3.8 TIMING AND CONTROL

3.8.1 GENERAL MEMORY TIMING

All timing generation circuits are located on the memory control card. The timing generation for all the various memory cycles, including refresh is centered upon a shift register, which consists of a number of D flip-flops arranged in such a way that it forms in principle a 7-bit shift register.
The timing edge sequence made with this shift register is in the first place designed such that the requirements of the 16K memory devices are fully met.
This shift register as a whole provides the multiple RAS (4x) and CAS (4x) pulses, which strobe respectively the row and column addresses into the memory devices (see also address selection and memory array), the address multiplex clock, and it provides also the timing for cycle and access control, refresh circuitry and data I/O control.
The clock for the shift register and other devices in the timing logic is provided by a 16 Mega cycle hybrid crystal oscillator which provides signals CL and CLN to the logic (after buffering) at 62.5 ns periods.
With reference to figure 3.19 General Shift Register Timing and the figure 3.20 Simplified Shift Register Circuitry it can be seen that at the start of a cycle all shift register -'Q'- outputs are in the low state. (Logical feedbacks over the shift register are in such a way that it is assured that the shift register will enter this state after the first refresh cycle after power up.)
This means that until CYREQ goes high none of the outputs are active.

CYREQ as will be seen later is activated either:

a. - By a Refresh, signal RFCYN (Refresh Cycle Not)

or b. - By a Read/Write request made by TMRN resulting in the activation of signal RWCYN (Read/Write Cycle Not).

On the next clock following the activation of CYREQ, the RASo output goes high. The addresses will already be presented to the address multiplexors and the row addresses (MAL07-14) selected, so the RAS signal (Row Address Strobe) will strobe the row address into the selected bar of 16K devices of the memory array. One clock later the signals MX. (multiplex) become high and will select the address inputs MAL 01-08 as memory device address. On the following clock, CAS strobes this column address into the memory devices selected by RAS. (Although CAS is given to all memory devices in the array only the selected devices by RAS-N, will strobe in the column addresses). The start of CAS on the memory devices is the time reference for the access time of data out.

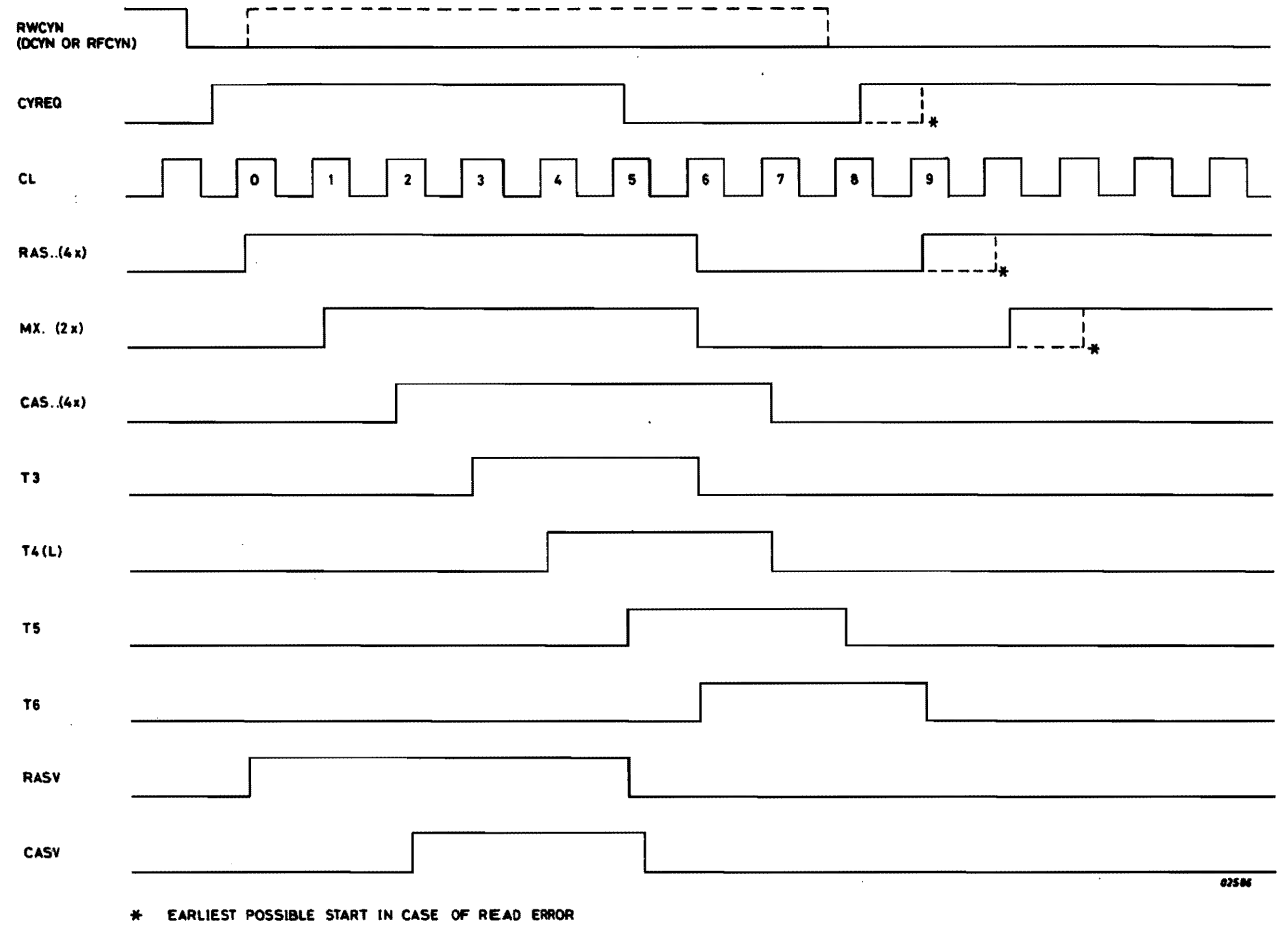


Figure 3.19 GENERAL SHIFT REGISTER TIMING

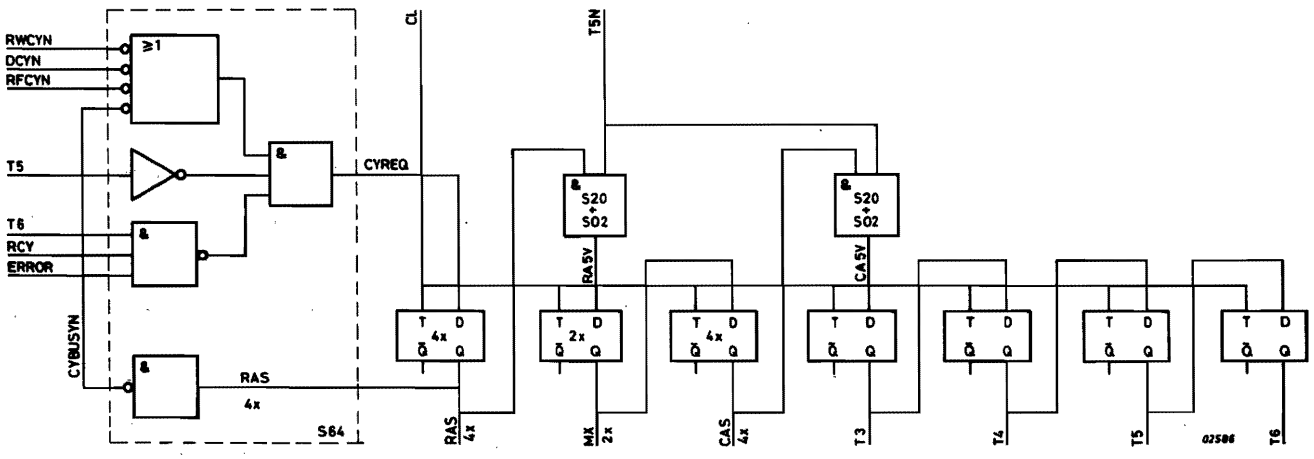


Figure 3.20 SIMPLIFIED SHIFT REGISTER CIRCUITRY

By the feed back of RAS as CYBUSN (Cycle Busy Not) to the input of the shift register, CYREQ remains active, so the read/write request may become inactive without consequences for the internal memory cycle.
Now during successive clock periods, T3, T4(L), T5 and T6 become active. T5 becoming high indicates the end of the internal cycle.
Signals CYREQ, RASV and CASV will all become low, and on the next RAS.. clock, MX. and T3 become low, followed by CAS, T4, T5 and T6.
As soon as T5 is low again the start of a new internal cycle will be possible, except in a read cycle with error then a new cycle is allowed one clock later if T6 is low.

3.8.2 TIMING FOR AN ERROR FREE READ CYCLE

Timing for the different kinds of cycles is very similar, the obvious main difference being of course in the signals controlling the enabling and selection of the circuits which handle the data flow.
The following description is made with reference to figure 3.21 and sheet of the memory control card circuits, also the assumption is made that there is no refresh request and that the previous cycle is completely finished.
Prior to the start of a memory request by TMRN (Timing Master to memory) going low, the address and control signals have been activated and are valid for at least 20 nsec.
The address, control and also the write data latches were transparent until TMRN went low, now these signals are all latched until the end of the cycle indicated by TMRN or CYBUSYN.
As indicated already in table 2.1-Cycle Mode Control Signals-, the signals WRITE, CHA and MAD15 define the kind of cycle to be executed, these three signals are decoded to control data flow and cycle timing. In case of a read cycle data flow is equal for all three possible cycles except for driving the data to the UPL-bus by TRDOL/R).

- Data Control in Read cycle

  After CASN is activated (low) on the selected bar of the memory devices, the memory device output enters the low impedance state, but data out (MDOO0-15, S0-S4) is valid 165 ns after the negative edge of CASN.

  EMDO being high during T4 forces the transceiver into the driving mode and data is sent over the internal memory bus (MIOB00-15, S0-S4) to the memory control card.

  Data is now offered directly through the opened data out latches, the correction circuits and the bus transceivers to the UPL-bus for ultimate speed.

The data out latch is always open when RAS is active (high), except in a refresh cycle, so data is latched and stored from the end of RAS until the start of a new Read or Write cycle.
The correction inputs ((CDOO-15 (Correction Data)) for the correction circuits (exclusive or) coming from the error correction decoder, are initially set in the low state, and stay in the low state when no error is detected.
The ENERCN (Enable Error Correction Not) signal, which disables the error correction decoder, S138 and 139 is reset at T3 true and is set at the leading edge of T4 when SF (Single Fail) is high. Under "NO ERROR" conditions, SF is low and ENERCH remains reset (High).
The bus driver to the UPL bus is forced into its low impedance state by TRDO(L/R) at T4, and will be disabled at the end of TMRN (going high). For control of TRDO(L/R) by means of CHA and MAD15, see table 3.1-Data Transfer Signals.
During a read cycle the WCY (Write Cycle) signal is low, which prevents enabling, of Data to the internal memory bus (MIOB) by the control card. WCY also enables the Data out S bits to the parity circuits (Syndrome bit generators - S280)

- Acknowledge Response to the UPL Bus
  TSMN - it indicates that the data out put on the UPL bus is valid on the master card. TSMN is given directly after the signal SF low is valid (no error).

  ACN . This signal is given at the begin of a Read (or Write) cycle and indicates to the master that the addresses and control signals are latched in, and no longer necessary for the memory.

3.8.3 TIMING FOR READ CYCLE WITH ERROR

Timing and control is as in an error free read cycle until the leading edge of T4.
An error in a Data or S bit will generate a syndrome bit (SEVO-4) code Unequal to all '1's. SF (Signal Fail) is high at the leading edge of T4 so after T4 both ENERCN (Enable Error Correction Not) and Error are active, low and high respectively.

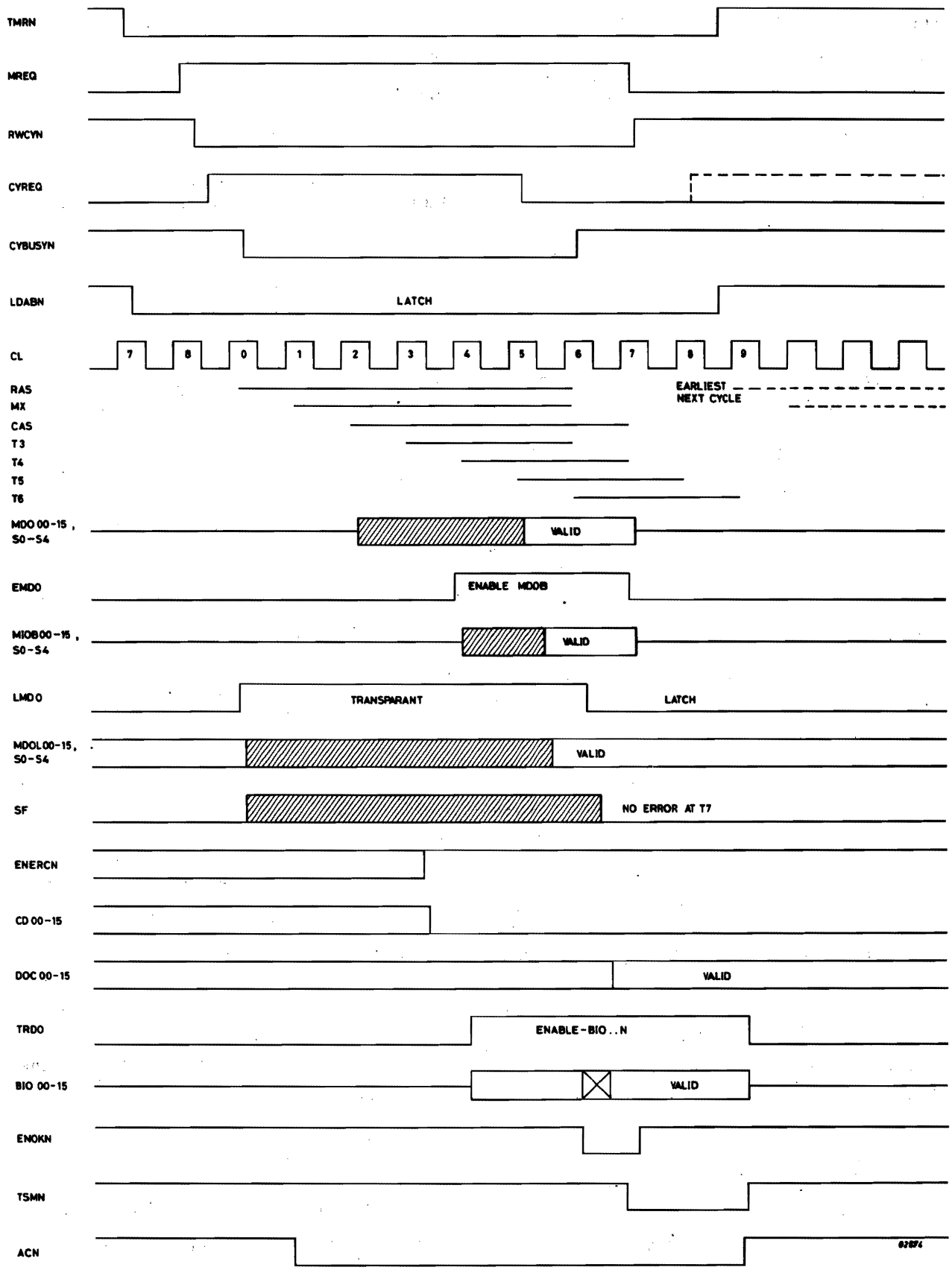


Figure 3.21 TIMING READ WORD/CHARACTER - NO ERROR

- Data Flow Consequences

The error correction decoder being enabled by ENERCN, low, will force one * of the CD00-15 signals high, (see also error correction circuitry), so the corresponding wrong data bit will be inverted by the correction circuit (74S86- Exclusive Or) that means data is corrected and is valid now after some propagation time on the Master.

* Note: In case of error in one of the check bits, all CD00-15 signals will become low after decoding.

- TSMN Consequences

SF being high at the leading edge of T4 (timing clock t7) prevents the generation of TSMN at that time moment as in an error free read cycle.
The signal ERROR enables now the generation of TSMN two clocks later (125 ns) when the corrected data is valid on the Master.

- Cycle Time Consequences

In case of error the off time between two cycles is stretched by one clock, by holding CYREQ low during T6, to prevent the premature start of a new cycle. This is necessary due to the fact that TSMN is delayed such that MREQ still asks for a cycle at the normal start point of a possible new cycle.

- Reset of ENERCN and ERROR

The reset of ERROR is always in the next cycle, however, if the next cycle is a refresh cycle a new TSMN would be generated without request.

On the other hand if a refresh cycle follows on a Read with error cycle the master may still require data, now ENERCN must stay active (low) while otherwise the corrected data would become uncorrected data again.

3.8.4 TIMING FOR A WRITE WORD CYCLE

The timing is very simular to the Error free Read cycle except of course the data control. Only the differences will be described.

- Data Control

Data offered by the UPL bus to the memory control card (BI000-15N) is gated through the bus transceivers and the transparent data-in latches directly to the internal memory data bus (MI0B00-15). Data-in is latched in with the same signal (LDABN) as address and control signals.

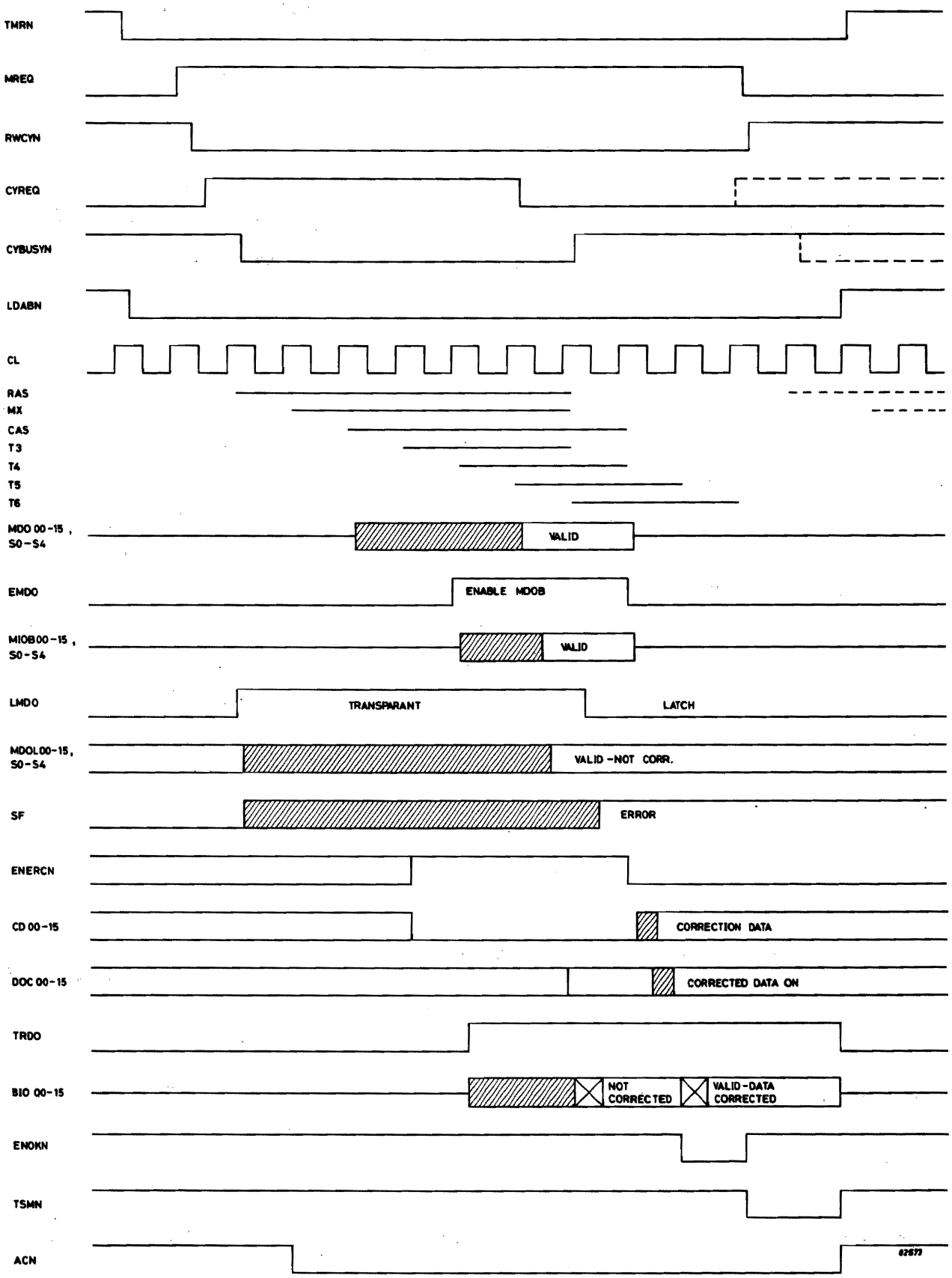


Figure 3.22 TIMING READ WORD/CHARACTER - ERROR

Data-in is also directed through the transparent data out latches to the parity circuits (= Check bit generation in write cycle). The check bit inputs (MDOLO-4) are all in the low state by WCY being high.
The output of the parity circuits, SEVO-4 are also offered to the internal memory I/O bus.
Both Data and S bits are now written into the selected address by WEN during T3 time.
Note that nearly all data control is by combinational logic and LMDO has equal timing for Read and Write cycles, the main difference is TRDO and WEN generation.

- Acknowledge response to the UPL Bus
  ACN is generated on the same time as in a Read cycle and also TSMN is given at that timing point, it indicates that all Data, Address, Write and CHA signals are not longer necessary.
  TMRN may become high now, and in theory also TSMN, but to prevent too small memory cycles on the UPL bus (which are not allowed!) TSMN high is delayed until the end of the internal write cycle.

3.8.5 TIMING FOR WRITE CHARACTER

RDCY is set by the leading edge of RAS if WRITEV and CHA are both high, and is reset also by the leading edge of RAS if RDCY is high.
The signal RDCY high during the first part of the cycle will have the following consequences.

- TMRN and ACN are given as in a normal WRITE cycle.

- WCY is held low so no data in can be put on the internal memory bus (MIOB) while EMDO is activated. So a normal Read cycle will take place, except that no TRDO is generated.

- LMDO is given to store the read and corrected data-out in an additional latch whose function is to feed back the data-out as data-in in the write part of the cycle.

- Also the second part of the cycle is initiated by RDCY by making DCYN low. (Double Cycle Not).

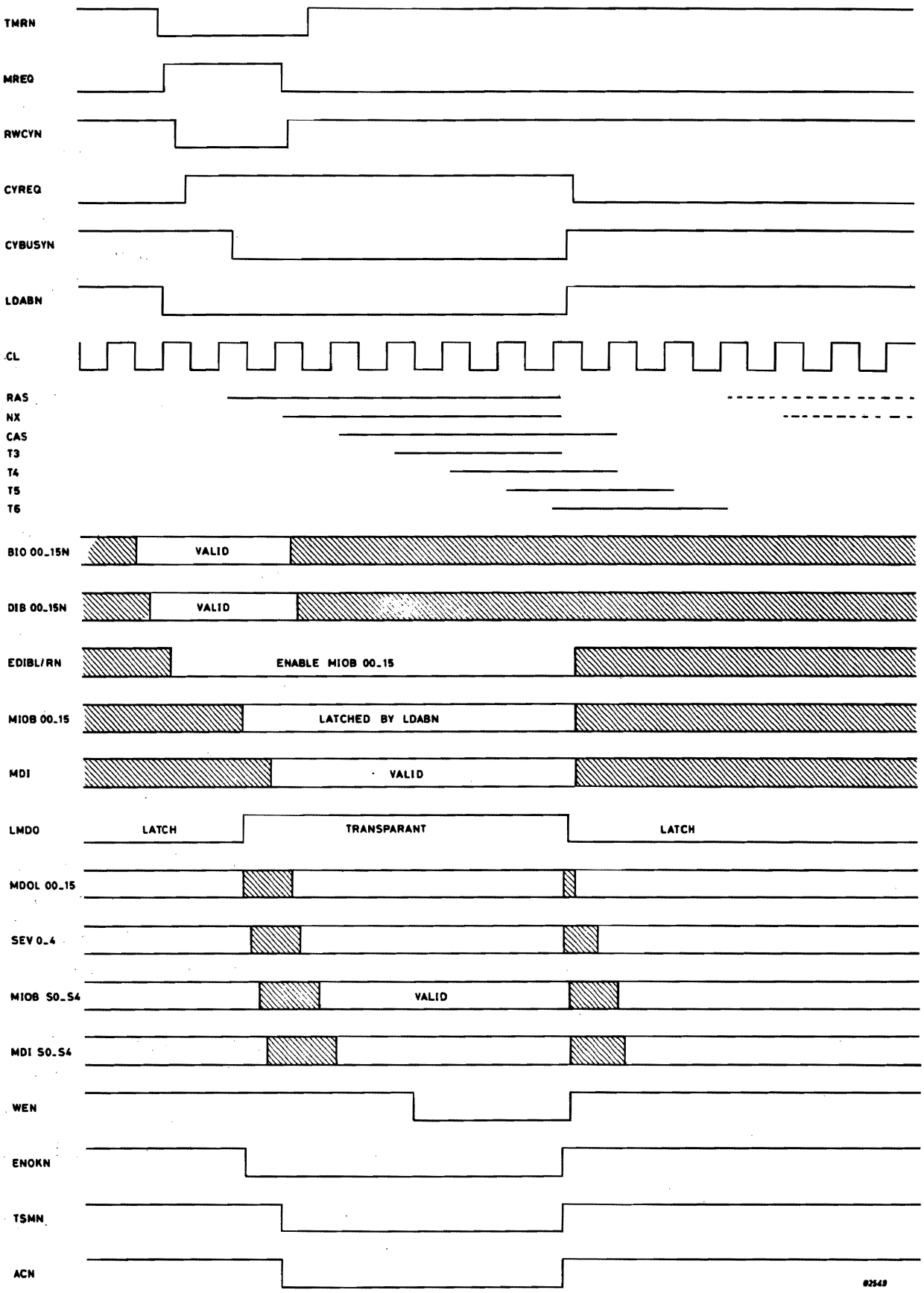


Figure 3.23 TIMING WRITE WORD

This latter signal also prevents the start of a refresh cycle after the first part of this Read/Write cycle.
The error correction decoder is enabled during the complete cycle (ENERCH low set by READ low) in order to have data corrected as soon as possible. (So no check for error, and no cycle stretch in case of error which are only possible in a normal 'Read' cycle.)
After the start of the second cycle part, RDCY is reset and now a normal Write cycle is performed, with Data to be written coming from an 'old' character and a 'new' character controlled by the bus enable signals ENI/O, BL/RN (Enable Data In/Out, Bus Left/Right Not).
TSMN is kept low during the complete Read/Write cycle by CYBUSYN, this latter signal being high from the start of RAS in the read cycle until the end of RAS in the write cycle.

3.8.6 TIMING FOR A REFRESH CYCLE

As stated before the 16K RAM's require complete refreshing (for all 16, 384 cells) within 2 ms. A refresh cycle differs from a normal read/write cycle in that the CASN signals are all held high (inactive) throughout the cycle. Thus the RAM's require only one 7-bit address, strobed by RAS, to refresh all 128 columns in the addressed row (the internal RAM cell array being 128 rows x 128 columns, figure 3.1 - Memory Device) the 128 columns are read out (each column having its own sense amp) and rewritten. This action restores the full charge which would otherwise leak completely away.

In a refresh action, then, it is required to refresh each of the 128 rows, in every RAM on all the cards, within 2 ms. With a clock period of 62.5 ns, 240 clock pulses elapse in exactly 15 µs; thus 128 x 15µs = 1.92 ms. So we require a counter which counts up to 240. If a refresh is performed at every count 240 = 15 µsec then the memory will be refreshed satisfactorily. However, if a refresh is performed at the end of every 15 µsec period indicated by STRF (STart ReFresh) there is a strong possibility that a refresh request may clash with a read/write request. As far as the refresh cycle goes, it is not important to wait even 1.1 µs for a Write character cycle to take place - it will still be possible to refresh within the 2 ms limit.
But the whole U.P.L. Bus will be held up if a master has to wait 560ns max. for a refresh to take place, hence the need for the two types of refresh.

There are two types of refresh cycle, known as Automatic Refresh (A.R.) and Hidden Refresh (H.R.) and their relation can be seen in figure 3.25, Refresh Relationship.

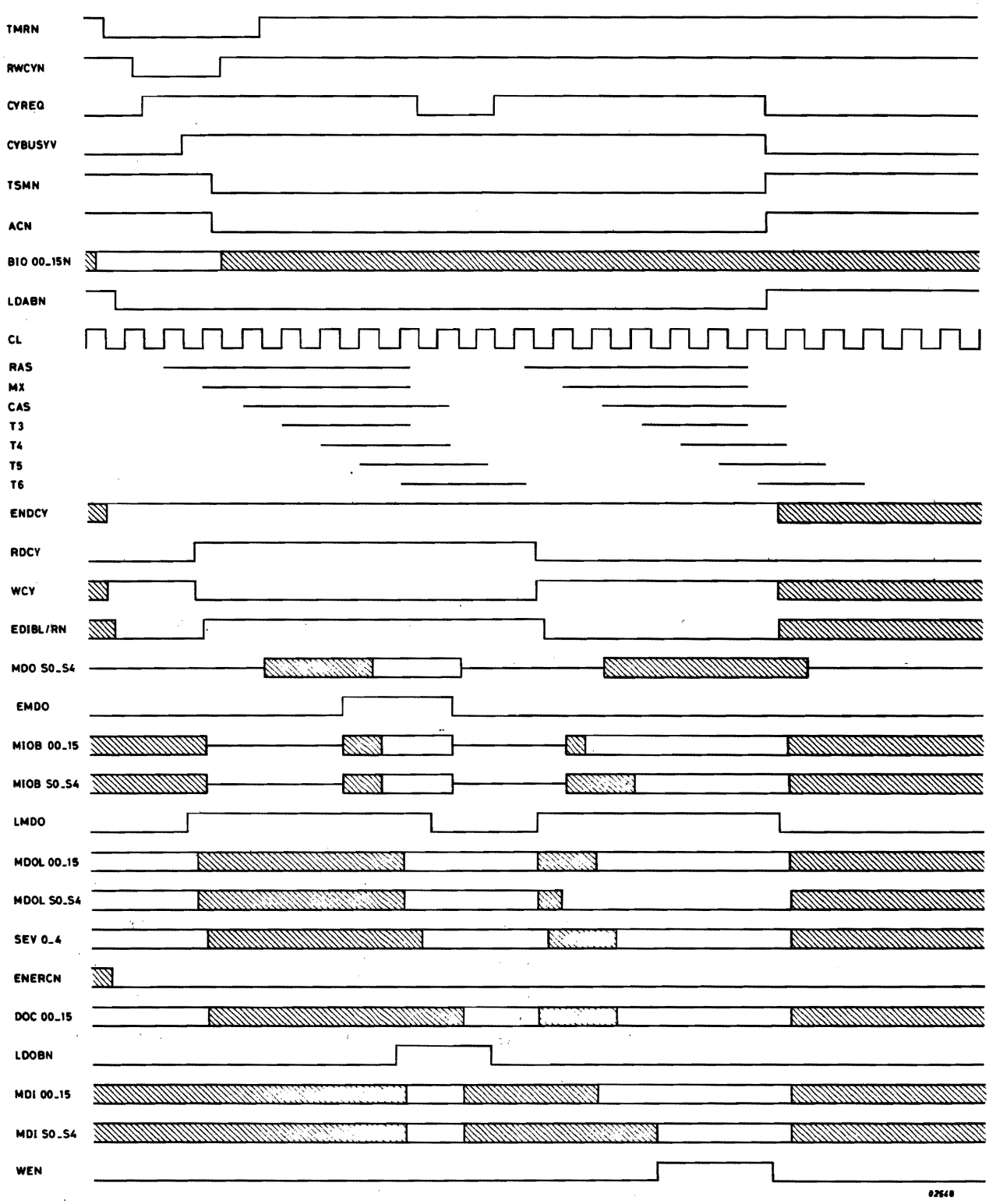
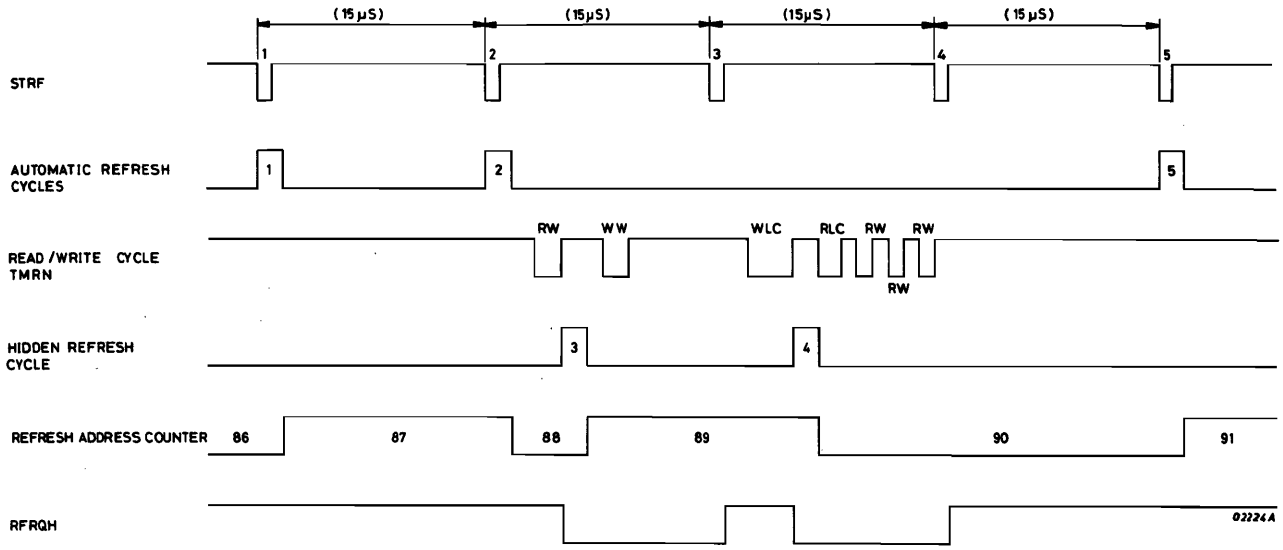


Figure 3.24 TIMING WRITE CHARACTER



RW = READ WORD
RLC = READ LEFT CHARACTER
WW = WRITE WORD
WLC = WRITE LEFT CHARACTER

Figure 3.25 REFRESH RELATIONSHIP

The definitions are as follows:

1. Automatic Refresh

   If there is no read/write request during a 15 μs period between two "STRF pulses" then a refresh is performed at the end of the 15 μs period as in "2" and "5" in figure 3.25. This is called an Automatic Refresh (A.R.).

2. Hidden Refresh

   If there is a read/write request during a 15 μs period between two "STRF pulses" then a refresh is performed immediately after the first (and only the first) read/write cycle and the A.R. at the end of the 15 μs period is disabled as in "3" and "4" in figure 3.25. This is called Hidden Refresh (H.R.) because the refresh can usually be performed before the master can respond to the TSMN and reactivate the TMRN for another read/write cycle.
   When the memory is busy, therefore, the chance of a master having to wait for the memory to perform a refresh is negligible.

The refresh addresses are completely independent of the read/write addresses and are provided by a Refresh Address Counter which increments the address by "1" at the end of every refresh.

Note that, in figure 3.25 although the refreshes occur at irregular intervals (1 - 2 = 15 µs, 2 - 3 ≈ 3 µs, 3 - 4 ≈ 16 µs, 4 - 5 ≈ 26 µs) there are exactly the same number of refreshes as STRF pulses because when an H.R. is performed, the subsequent A.R. is not, so only one refresh occurs in every 15 µs period.

The refresh period is timed by Refresh Counter which consists of two 4-bit counters linked so that every time counter 1 reaches 16 (the transition from "1111" to "0000") counter 2 is clocked.
Counter 1 is clocked by CLN every 62.5 ns so counter 2 is clocked every 1 µs.

When counter 2 reaches "1111" the signal RPCAR1 (Refresh Period Carry 1) goes low via a NAND and, two clocks later as RPCNT1 goes high (count 2 of counter 1), a D-type flipflop is clocked to force STRFN (Start Refresh Not) high and STRF low. STRFN going high clocks counter 2 to "0000" (thus counter 2 counts from "0001" to "1111" which is 15) and STRF going low clocks a JK flipflop with RFRQH as its "J" input. As we shall see later, if there has been a read/write request during the previous 15 µs period, then RFRQH (Refresh Request Hidden) will be low thus preventing the A.R. from continuing any further. If, however, there was no R/W cycle during the previous 15 µs period then RFRQH is high and the flipflop forces ERFRQN (Enable Refresh Request Not) low.
At this moment we can assume SARFRQN (Set Advance Refresh Request Not) to be high (inactive) as will be shown later. Therefore, via a NAND gate, JRFRQ (J Refresh Request) goes high. At the next CLN. JRFRQ forces ARFRQ (Advance Refresh Request) high and, again one CLN later, RFRQ (Refresh Request) goes high. (Refer to Memory Control Card).

At this point, the refresh may be held up if a R/W cycle is taking place, or is about to take place by an AND gate with inputs RWCYN (Read/Write Cycle Not - inactive high), CYBUSYN (Cycle Busy Not - inactive high) DCYN and RFRQ. If all is well, RFE (Refresh Enable) goes high and, in successive clocks, ARFCY (Advance Refresh Cycle) and RFCY (Refresh Cycle) both go high. ARFCY going high disables the R/W Address Multiplexor, ARFCYN going low enables the Refresh Address Counter address to the memory array as A (0-6), RFCYN going low enables all the RAS N strobes on memory slave cards while RFCYM (basically the same signal) forces CASN all high. RFCYN going low also forces CYREQ high and starts up the shift register.

The clock timing is exactly the same as for a normal "short cycle" but the RAM's realise this is a refresh and not a R/W cycle because CASN (0-3) are held high throughout the cycle.
Of course no TSMN or TRDO is generated in this Read/Refresh cycle.
Meanwhile, STRF has gone high again as the flipflop "resets" due to RPCAR1 being high (counter 2 having been reset as described previously) and RPCNT1 going high at count 6 of counter 1. STRF going high clocks another D-type flipflop to ensure that RFRQH (Refresh Request Hidden) is high. Note that, as this description applies to an A.R. then RFRQH would be high anyway since there would have been no R/W cycle to reset it (described below). Had STRF pulse followed a period during which there has been a R/W cycle. RFRQH would be reset at this time to enable a H.R. during the reset 15 µs period.
The A.R. would then be disabled as previously described.

The A.R. cycle ends as follows. ARFRQ is reset as the ARFCY flipflop sets (due to ARFCYN going low). ERFRQN and RFRQ are reset at T5 by RRFRQN (Reset Refresh Request Not). RFE is reset (made low) by RDRQ, and ARFCY follows one clock later. RFCY is reset by CAS going low, forcing RRFCYN (Reset Refresh Cycle Not) low and resetting the flipflop. If, during a refesh cycle a R/W request became active due to TMRN going low, it is held up by RFRQN being low. But RFRQN goes high (thus enabling RWCYN to go low) before RFCYN goes high, thus CYREQ remains high and the R/W cycle takes place one clock later.

As this R/W cycle is now the first of the new 15 µs period it generates a H.R. as follows. At time T3 of the R/W cycle, SARFRQN (Set Advanced Refresh Request Not) goes low due to all four NAND inputs being high (RFCYNV because it is not a refresh cycle, RFRQH because it either was high already or was set at the last STRF pulse, T3 from the shift register and DCYN which just prevents the refresh from occuring between the two cycles of a Write Character Operation). SARFRQN going low enables JRFRQ via a NAND (ERFRQN is high at this time) and so begins the sequence of events already described leading up to a refresh cycle immediately following the R/W cycle. However, when ARFRQ becomes high, RRFRQHN (Reset Refresh Request Hidden Not) goes low (ERFRQN is still high) thus resetting RFRQH and disabling the NAND so that any further R/W cycle will not enable SARFRQN and so start refresh cycles.

RFRQH now remains low until the next STRF pulse at which no A.R. is generated (because RFRQH is low) but then RFRQH is reset to enable the H.R. for the first R/W cycle of the following 15 µs period.

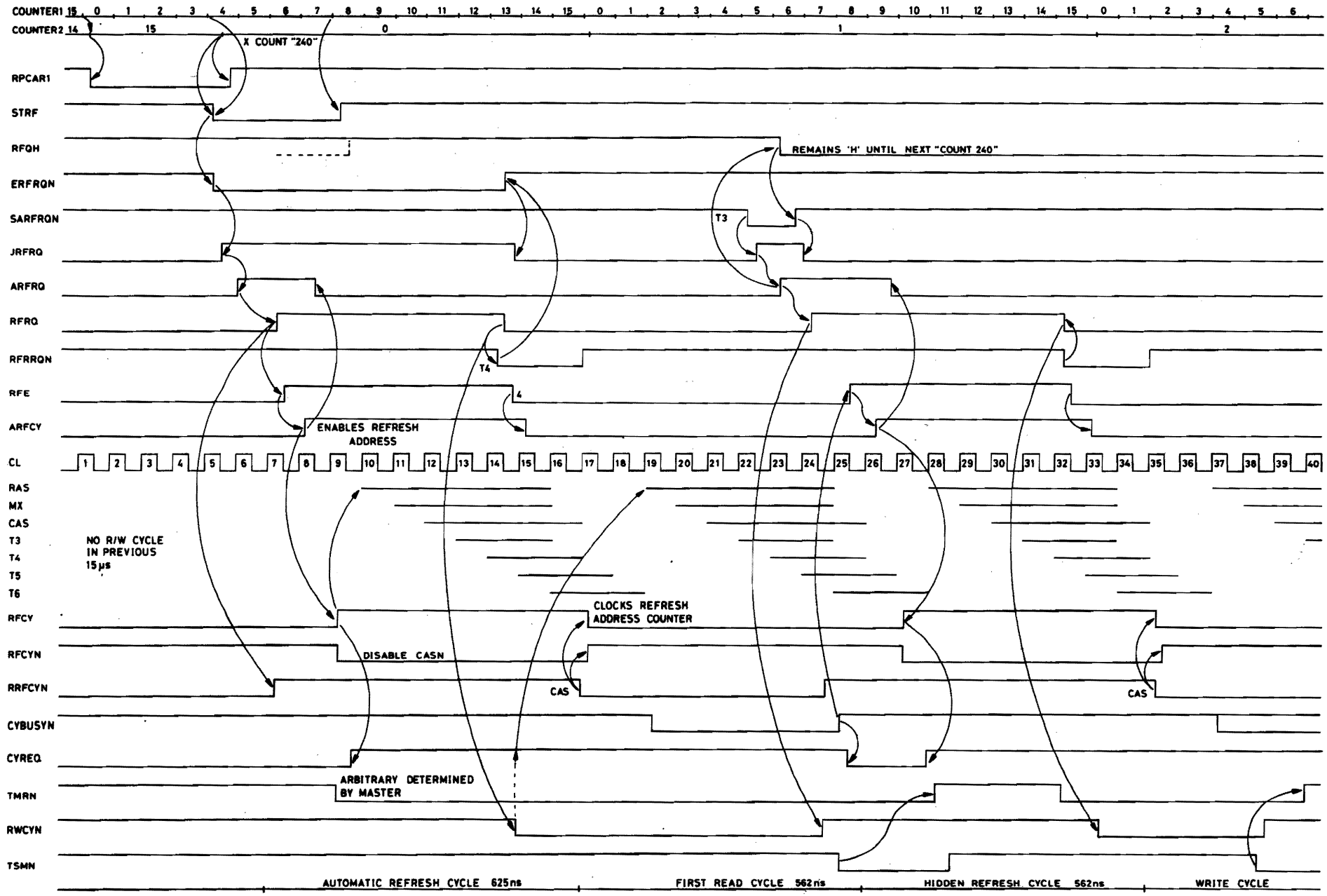


Figure 3.26 REFRESH TIMING

3.9 MISCELLANEOUS CIRCUIT DESCRIPTIONS

3.9.1 POWER SUPPLY AND BATTERY BACK UP

As described in section 1.3.2 the memory is supplied with two +5 Volt supplies, one for the circuits which must stay on in case of power break down, called B5PU (B is for Battery) and one for the other circuits called P5PU (P is for Power). The +12V supply for the memory is also a battery backed power supply. B12P to supply the memory devices themselves

During normal system operation all supplies are valid and the RSLN (Reset Line Not) signal is high.

In the power/battery stand by mode respectively, due to machine switch off or power break down, the RSLN signal will become low to indicate that power is down. This forbids the start of any new cycle except Refresh cycle of course, and sets control signals.

After RSLN low, the P5PU will be switched off while the B5PU and B12P will be kept valid either by a separate power supply directly connected to the mains or by battery back up.

All devices marked with a 'B' in a corner are connected to the battery B5PU and memory devices also to B12P.

With reference to the circuits it can be seen that all the refresh and addressing logic is still working and that the data I/O circuitry and their related timing and control circuits are down.

By means of this stand by/battery option, information of the memory is not lost in case of power down while power consumption is reduced to a minimum.

3.9.2 DECOUPLING OF THE MEMORY ARRAY

Although the number of decoupling capacitors in the memory array is less than suggested by the device manufacturers for dynamic memory arrays on double sided prints, the high frequency interference is well within limits due to the multilayer board.

3.9.3. +12V to -5V CONVERTER

On every memory slave card a +12V to -5V converter is placed. In this way no problems will arise if:

a) The memory control card is removed and power is applied to the system, (no open -5 Volt supply).

b) A short circuit on the backpanel to the -5 Volt would occur.

3.9.4 REDUNDANT CIRCUITRY

The RAS outputs (4x) of the shift register (74S174) are the first signals after the synchronisation circuitry, due to this there might be a possibility* that in case of very long metastable times of the synchroniser flipflop (7S74) not all four RAS signals become high after the clock.

To avoid timing problems for the memory devices the MX signal is not generated as long as not all RAS signals are high (AND on RAS signals enables MX on the next clock).

On the other hand, to avoid to early break off, of the cycle, the CYBUSYN signal is generated as soon as one of the RAS pulses is high (OR on RAS signals).

So these OR and AND functions will only have a logical function in case of RAS synchronize problems.

* Possibility of this kind of synchronize problems worst case once every month.

3.9.5 PULL UP RESISTORS

A large number of pull up resistors are placed on the master control card to simplify testing of the card on the General tester.

Special attention is paid for test points and logic design for testability of redundant circuits.

3.9.6 STAND BY MODE

To prevent possible interference to the timing and refresh circuitry from switched off Data control circuits in case of power break down, a number of timing signals are generated separately to the logic and battery supplied TTL circuits (T4L = T4 logic, RFCYNL = Refresh Cycle Not Logic).

On other places TTL gates connected to the battery supply, are used as a logic buffer between timing and control circuits (on the battery supply B5PU) and other circuits (on the logic supply P5PU).

3.10 HIGH SPEED VERSION

The differences for the High Speed Version with respect to the standard version, are listed below:

. Memory Slave Card WMB1

High speed memory devices are used, with an access time of 100ns in stead of 165ns (referred to CAS).

. Memory Control Card WMC

Timing is speeded up by applying a X-tal with a higher frequency.

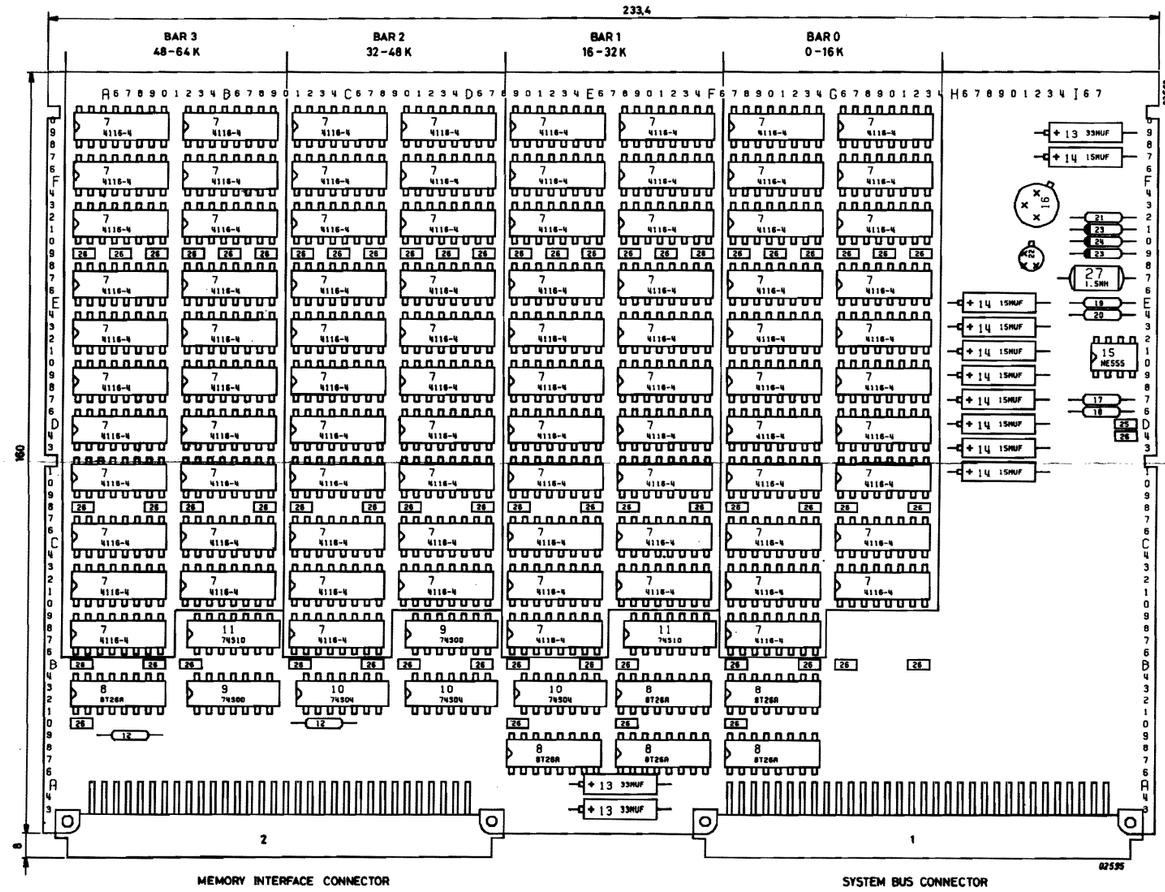
- Frequency : 18,43 MHz i.s.o. 16 MHz
- Clock period: 54.25 µsec. i.s.o. 62.5 µsec.

Read Access is shortened by generating earlier the TSMN signal.

- Timing signals T4 and T6 for the generation of ENOKN are replaced by T3 and T5.
- Timing signal T3 for the generation of MDO is replaced by MXR.

To speed up the data transfer during a character cycle the latches 74 LS 373 on locations C9B8, E0A8, C9A8, E0B8, (figure) are replaced by 74 S 373 IC's.

4 DIAGRAMS


233,4
BAR 3
48-64 K
BAR 2
32-48 K
BAR 1
16-32 K
BAR 0
0-16 K
100
MEMORY INTERFACE CONNECTOR
SYSTEM BUS CONNECTOR

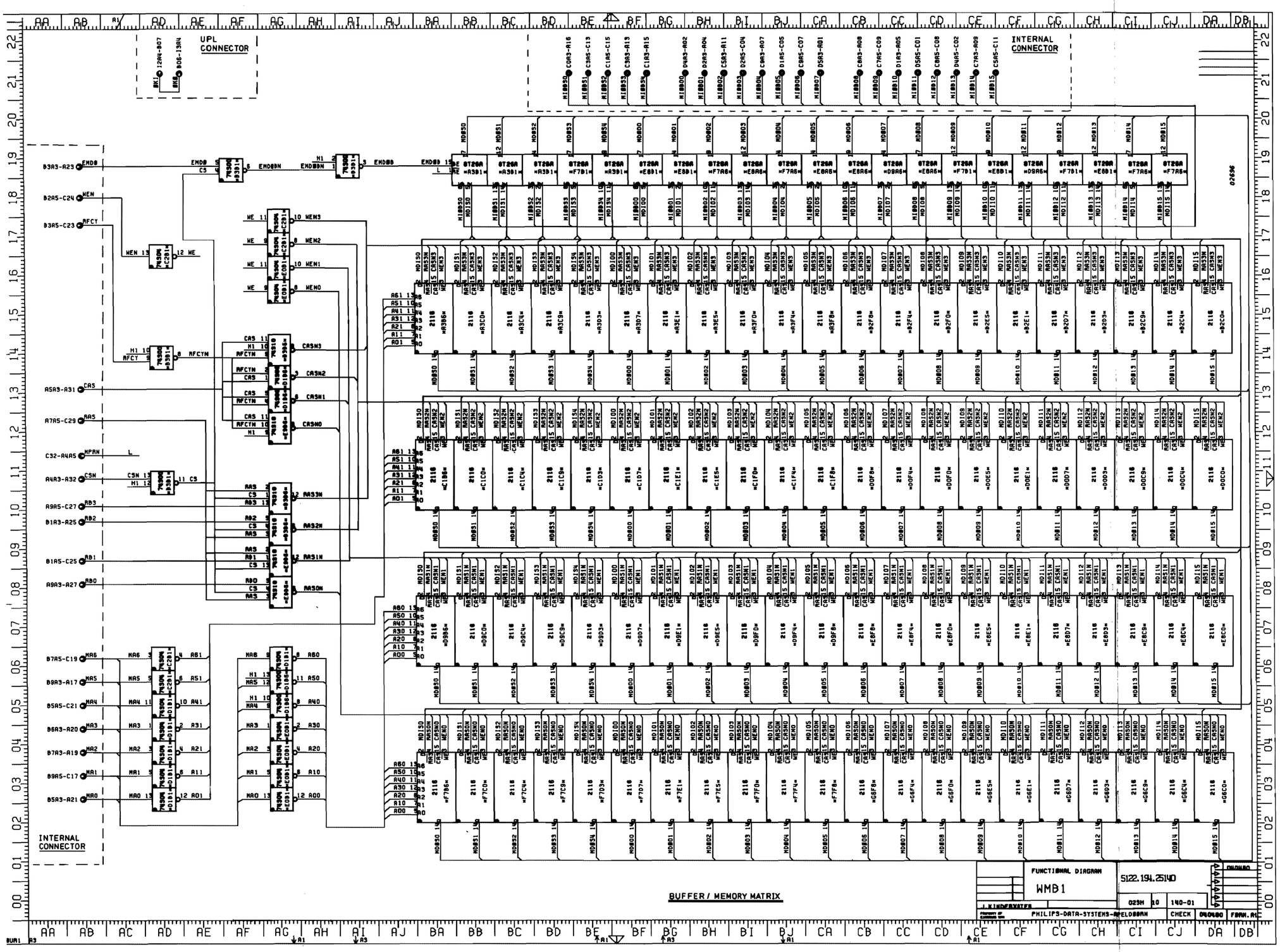


Figure 4.1 BUFFER/MEMORY MATRIX (WMB1)

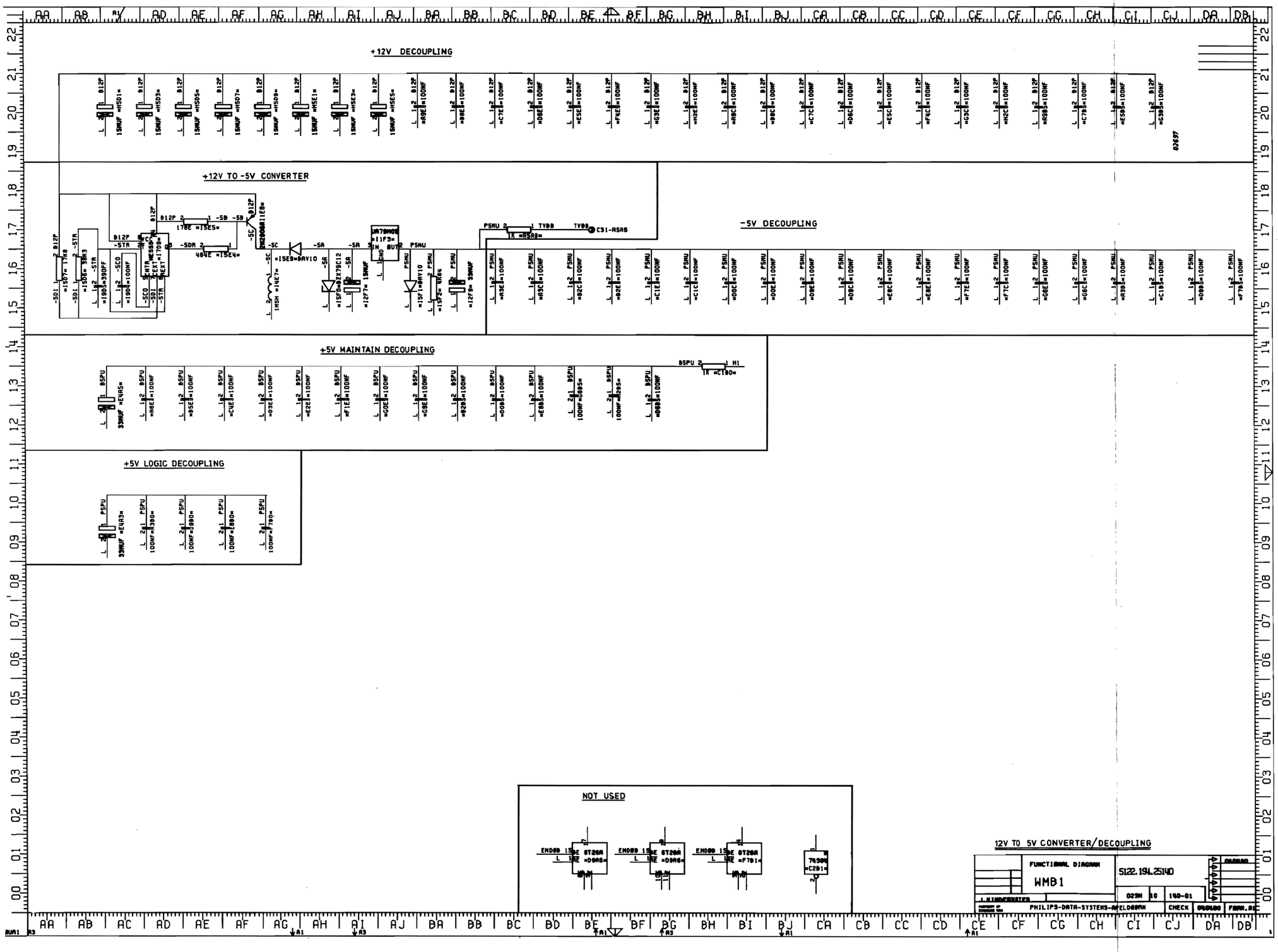
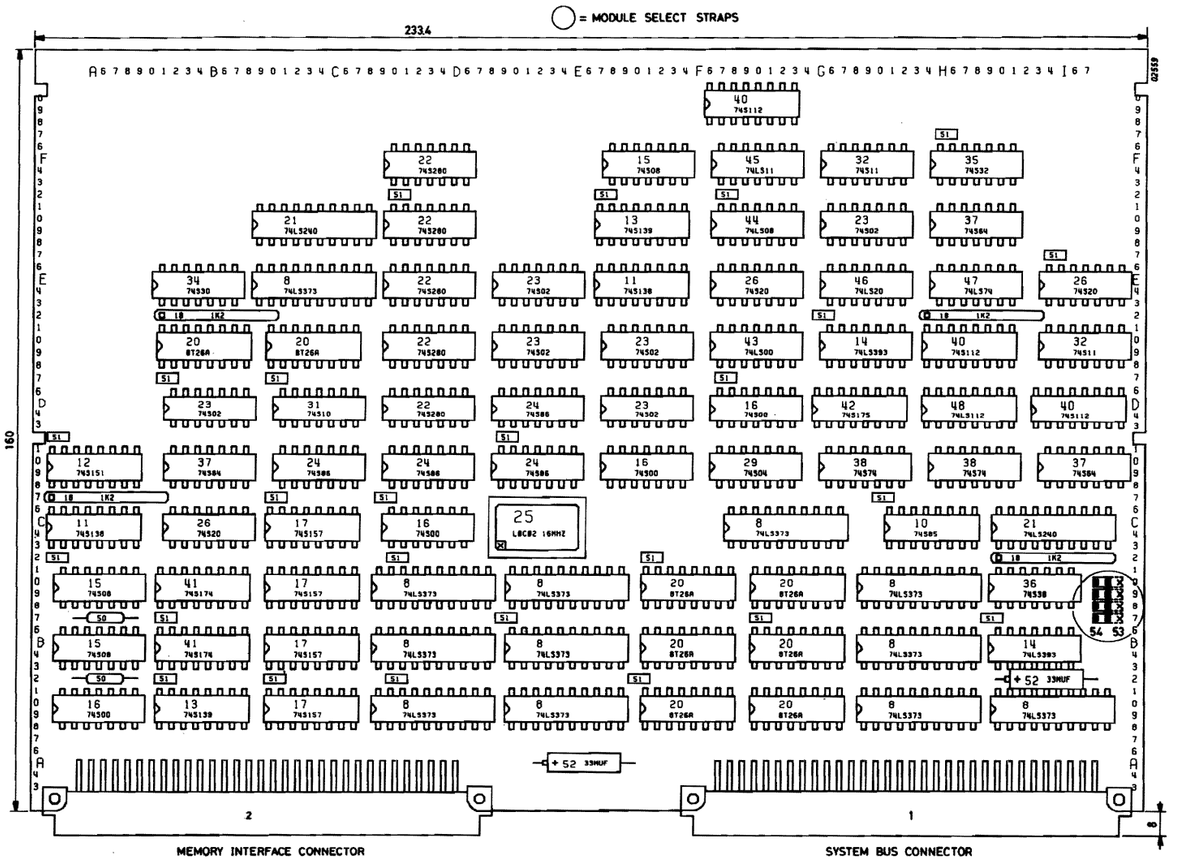


Figure 4.2 12V to 5V CONVERTER/DECOUPLING (WMB1)


○ = MODULE SELECT STRAPS
233.4
160
MEMORY INTERFACE CONNECTOR
SYSTEM BUS CONNECTOR

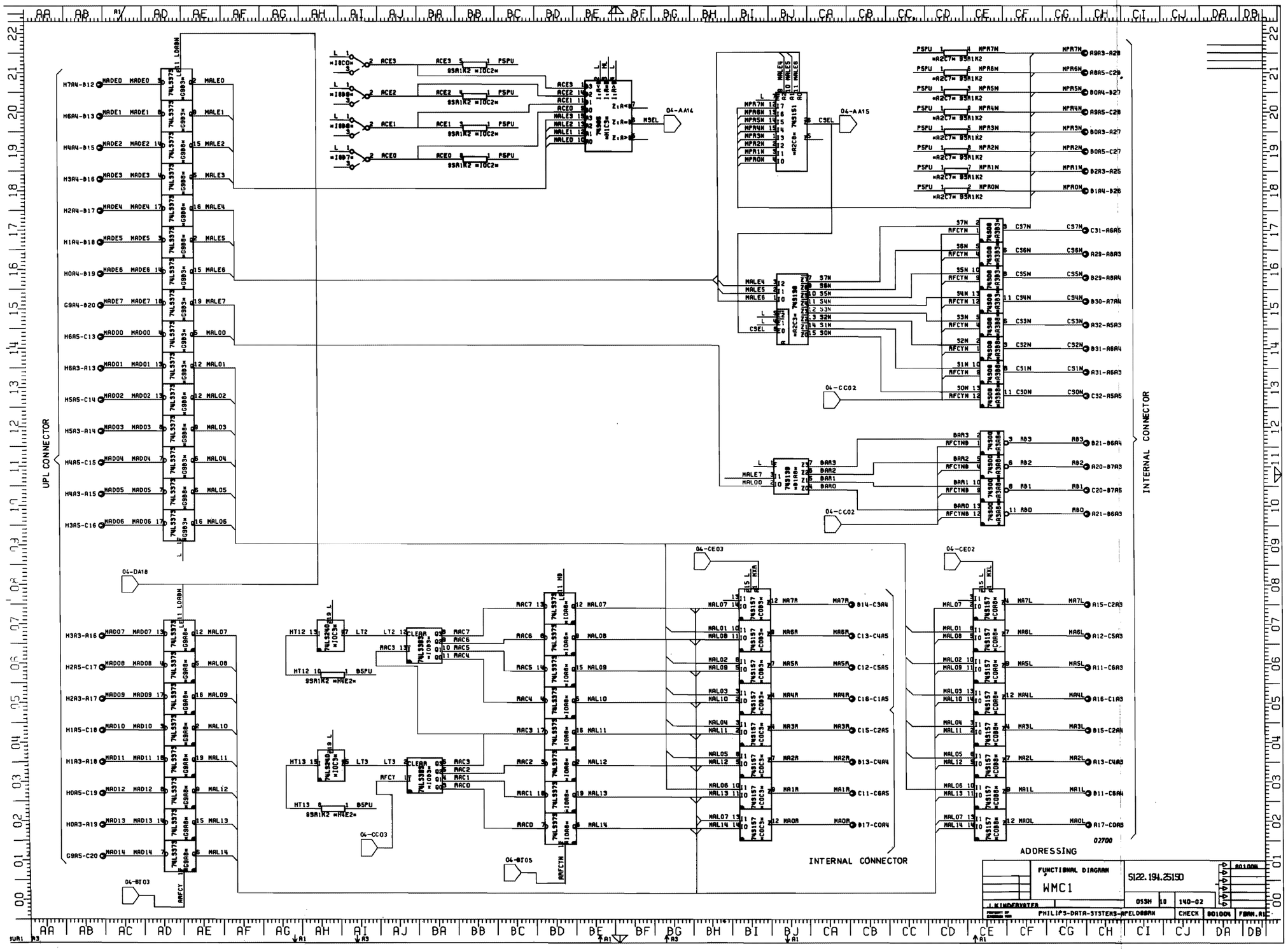


Figure 4.3 ADDRESS INTERFACE (WMC1)

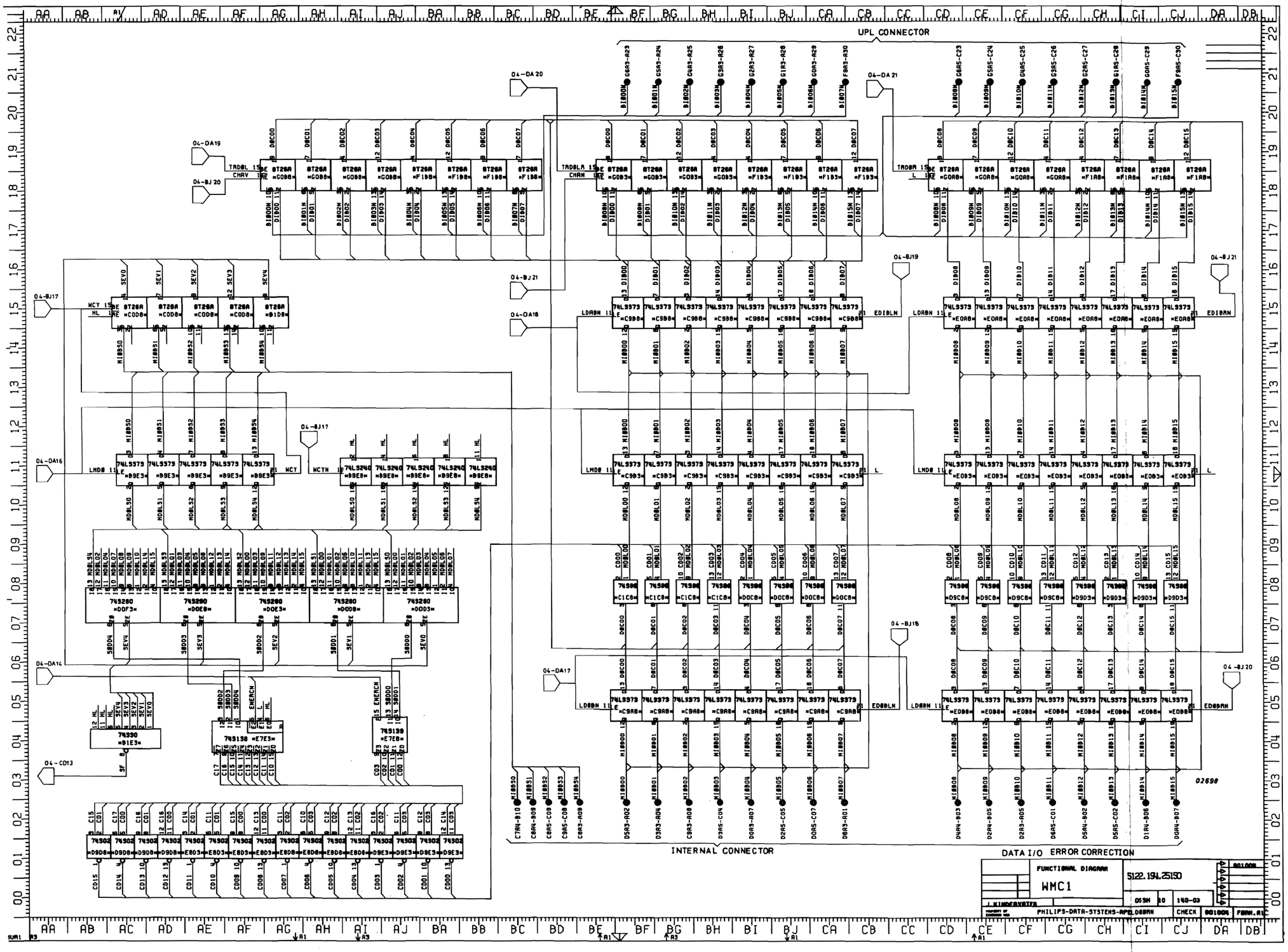


Figure 4.4 DATA I/O LOGIC

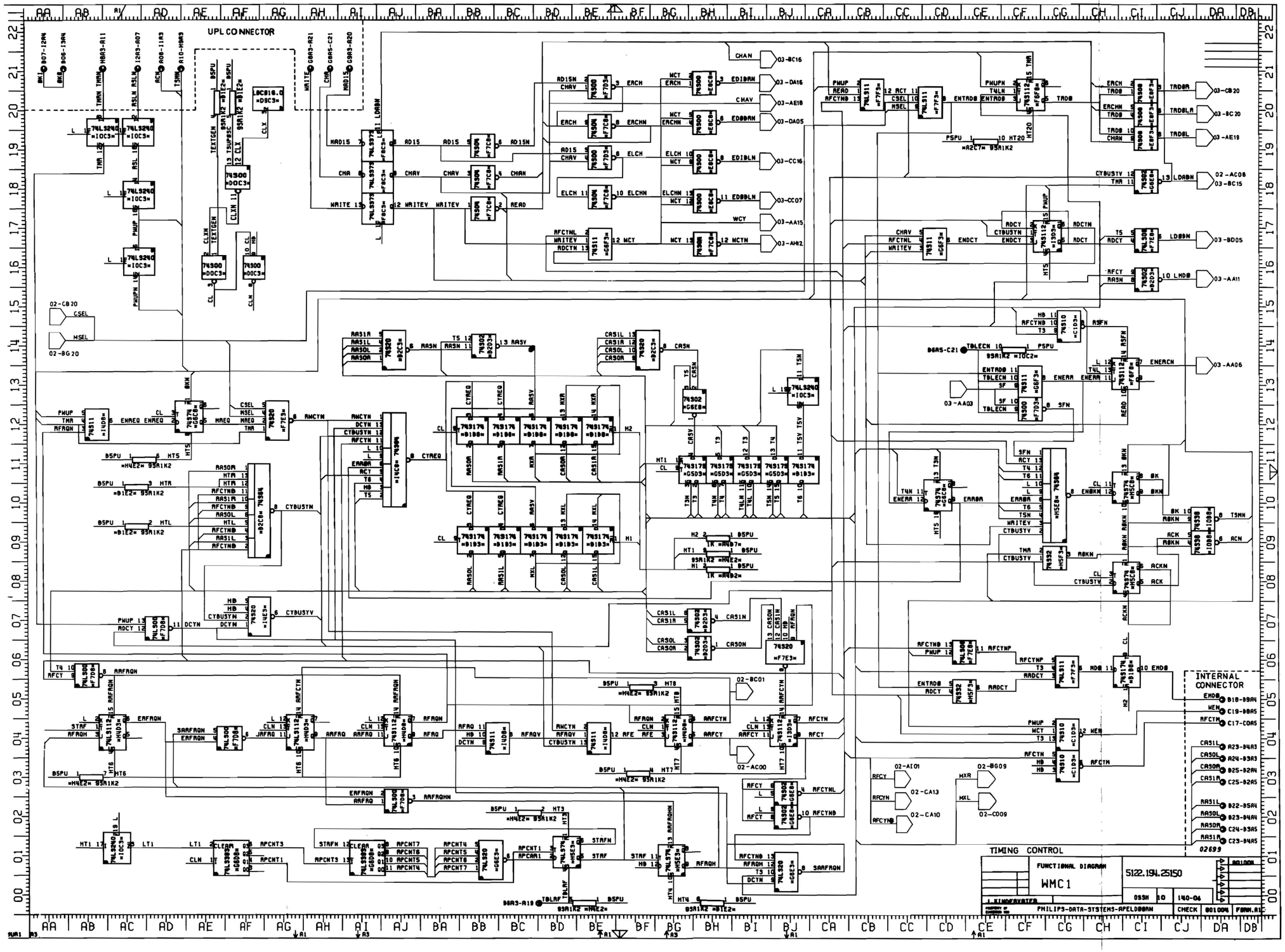


Figure 4.5 TIMING AND CONTROL (WMC1)

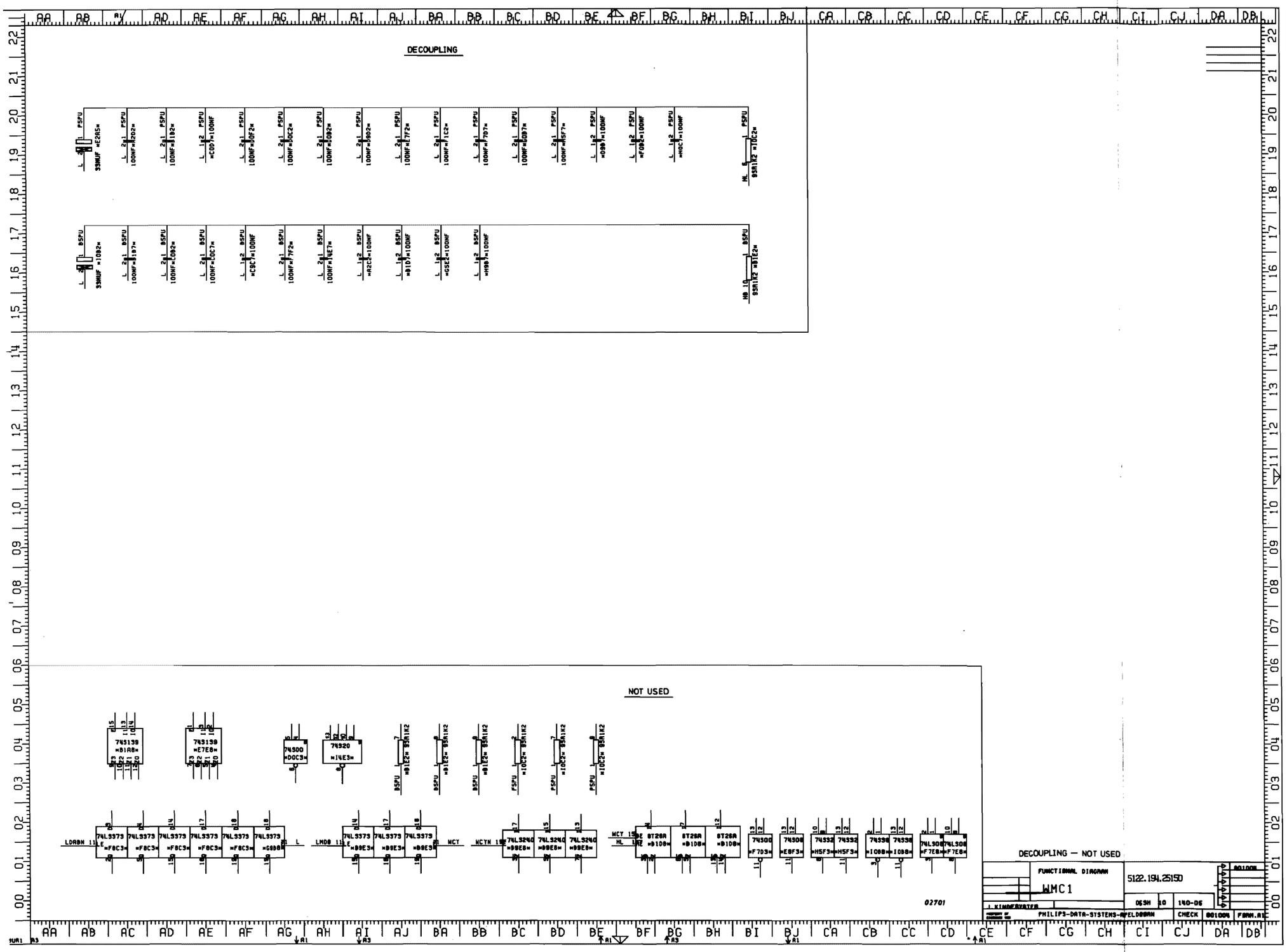


Figure 4.6 5V DECOUPLING + NOT USED (WMC1)

CARD PØSITIØN ØN BACKPANEL

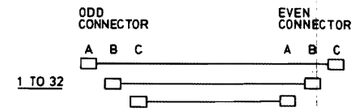
15	16	17	18	19	20	21	22	23
SLAVE7	SLAVE5	SLAVE3	SLAVE1	MASTER	SLAVE0	SLAVE2	SLAVE4	SLAVE6

SLAVE

MEMØRY SLAVE
CARD-WMB
512219425140

MASTER

MEMØRY CØNTRØL
CARD-WMC
512219425150

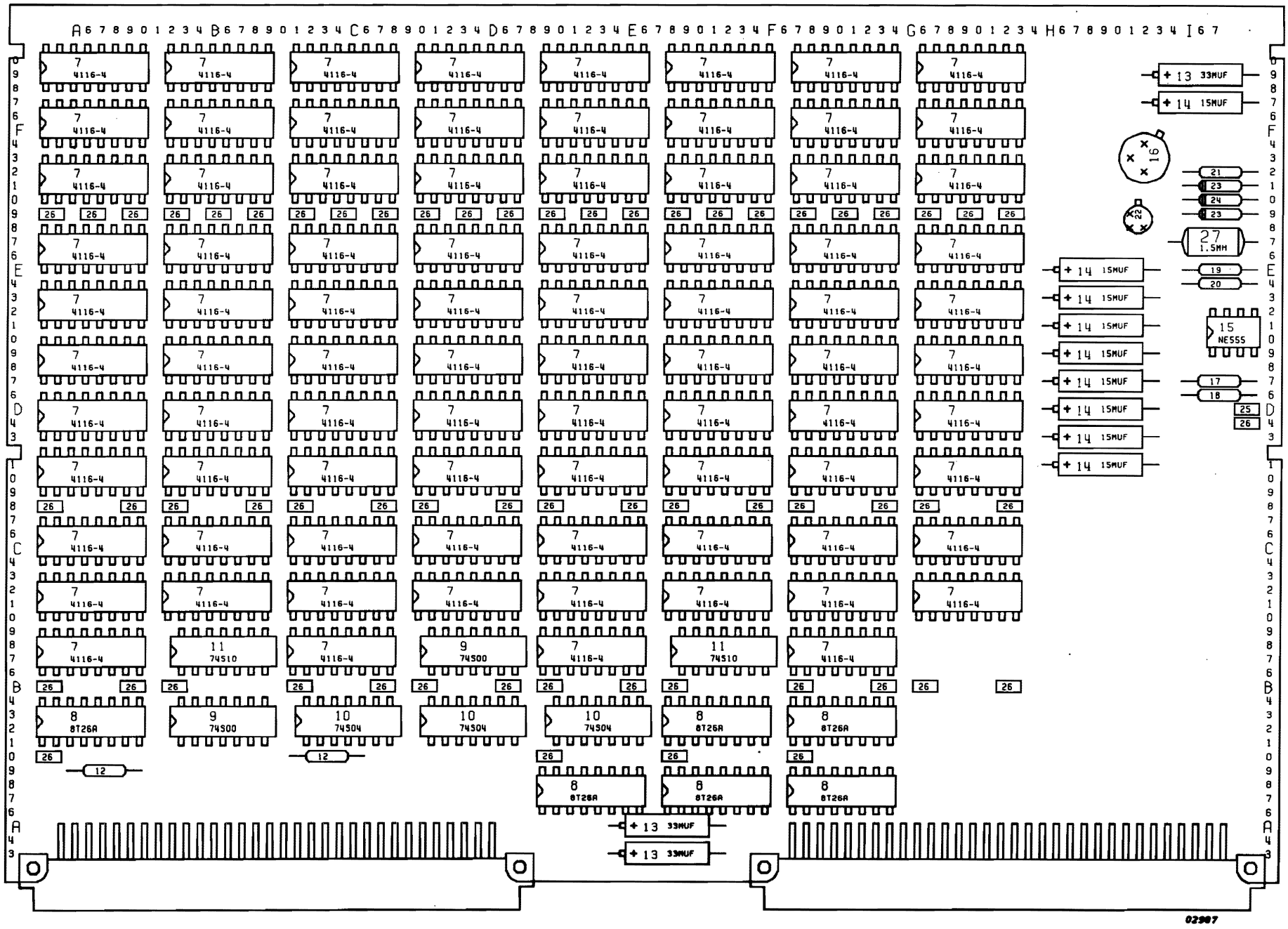


FROM CARD POSITION ON BACKPANEL 1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14, ARE THE LOGIC POINTS CONNECTED AS SHOWN.

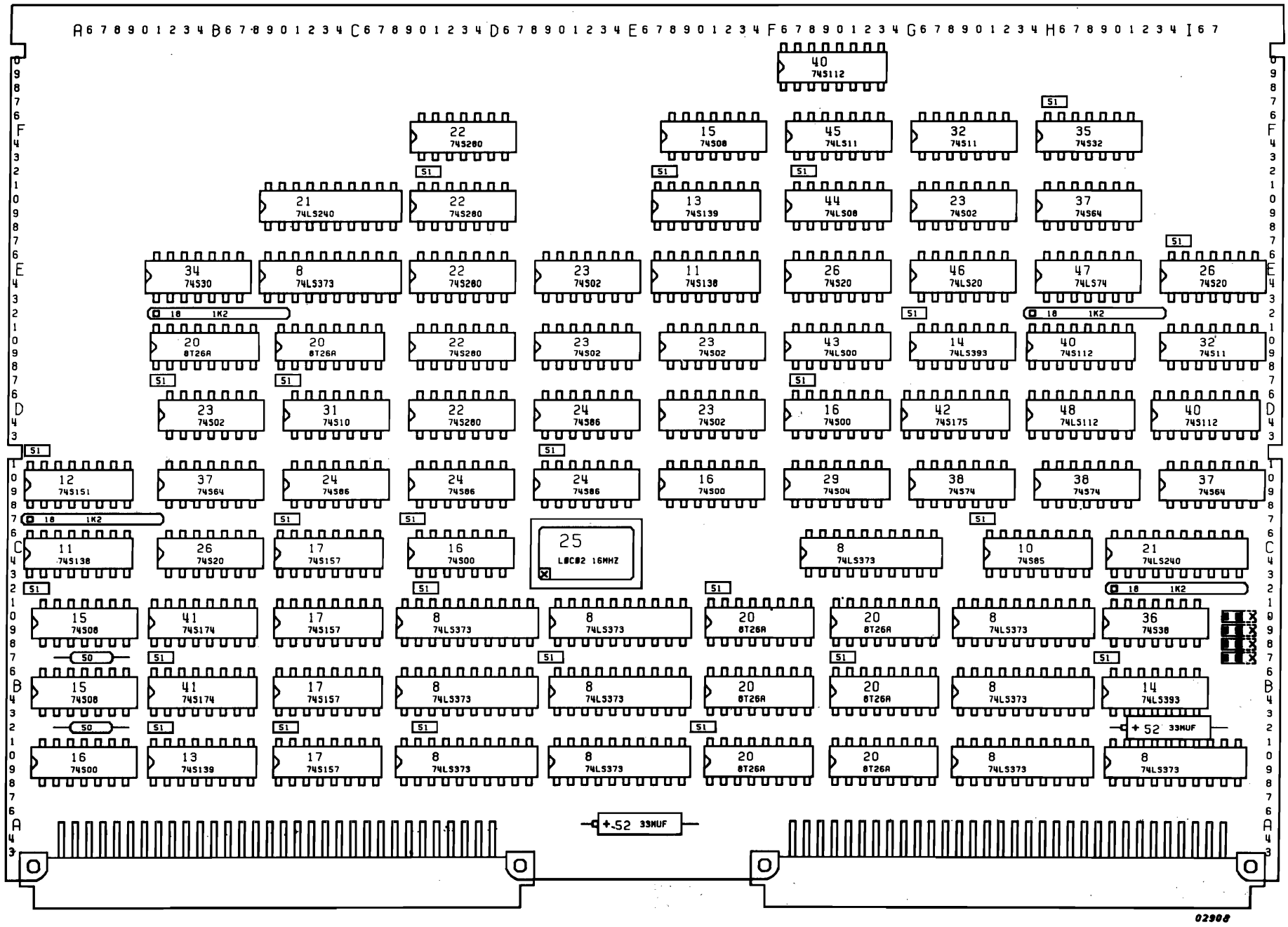
FUNCTIONAL DIAGRAM
WC1
5122.194.24490
PHILIPS-DATA-SYSTEMS-APELDOORN

Figure 4.7 BACKPANEL INTERCONNECTIONS (WMC1)

6 PARTS LIST


PCB WMB1
7 4116-4
11 74S10
9 74S00
10 74S04
8 8T26A
+13 33MUF
+14 15MUF
27 1.5MH
15 NE555
12
02907

Pos.	Code Number	Description
1A	5122 194 25140	PCB WMB1 compl.
2B	5122 000 11630	Connector MP F068-196C
3B	5122 000 11640	Connector MP F068-164C
7B	5122 194 26610	IC 4116-4
8B	5122 000 09520	IC 8T26
9B	5122 000 10080	IC 74S00
10B	5122 000 09820	IC 74S04
11B	5122 000 09490	IC 74S10
12B	2322 151 51002	Resistor 1K MR25
13B	2022 001 00142	Capacitor 33µF
14B	2022 001 00159	Capacitor 15µF
15B	5122 000 08810	IC NE555
16B	5122 000 09850	IC UA79M05
17B	2322 151 51783	Resistor 17K8 MR25
18B	2322 151 53833	Resistor 38K3 MR25
19B	2322 151 51781	Resistor 178E MR25
20B	2322 151 54641	Resistor 464E MR25
21B	2322 151 54642	Resistor 4K64 MR25
22B	9330 907 40112	Transistor 2N 2906A
23B	5122 000 05290	Diode BAV10
24B	9331 178 10112	Diode BZX79-C12
25B	2222 641 70391	Capacitor 390 pF 100V
26B	5122 000 11360	Capacitor 100 nF 50V
27B	4322 057 11521	Coil 1,5 MH
28B	2413 490 00009	Mounting pad TO 18
29B	4322 026 71861	Mounting pad TO 5


PCB WMC1
40 74S112
22 74S280
15 74S08
45 74LS11
32 74S11
35 74S32
21 74LS240
13 74S139
44 74LS08
23 74S02
37 74S64
34 74S30
8 74LS373
26 74S20
46 74LS20
47 74LS74
20 8T26A
43 74LS00
14 74LS393
40 74S112
32 74S11
31 74S10
24 74S86
16 74S00
42 74S175
48 74LS112
12 74S151
29 74S04
38 74S74
41 74S174
17 74S157
36 74S38
10 74S85
25 L@C@2 16MHZ
1K2
S1
S0
+52 33MUF
02908

Pos.	Code Number	Description
1A	5122 194 25150	PCB WMC1 compl.
2B	5122 000 11630	Connector MP F068-196C
3B	5122 110 91490	Oscilator foot
8B	5112 000 10130	IC 74LS373
10B	5122 000 09240	IC 74S85N
11B	5122 000 09250	IC 74S138
12B	5122 000 09510	IC 74S151
13B	5122 000 10870	IC 74S139
14B	5122 000 10760	IC 74S393
15B	5122 000 10800	IC 74S08
16B	5122 000 10080	IC 74S00
17B	5122 000 09500	IC 74S157
18B	5122 000 11560	IC 9SR1K2
20B	5122 000 09520	IC 8T26
21B	5122 000 10600	IC 74LS240
22B	5122 000 10120	IC 74S280
23B	5122 000 10780	IC 74S02
24B	5122 000 10040	IC 74S86
25B	5122 000 11320	LOCO 16,0
26B	5122 000 10100	IC 74S20
29B	5122 000 09820	IC 74S04
31B	5122 000 09490	IC 74S10
32B	5122 000 10090	IC 74S11
34B	5122 000 10810	IC 74S30
35B	5122 000 10820	IC 74S32
36B	5122 000 09960	IC 74S38
37B	5122 000 09650	IC 74S64
38B	5122 000 10110	IC 74S74
40B	5122 000 09700	IC 74S112
41B	5112 000 09600	IC 74S174
42B	5122 000 10900	IC 74S175
43B	5122 000 09120	IC 74LS00
44B	5122 000 09660	IC 74LS08
45B	5122 000 09130	IC 74LS11
46B	5122 000 09140	IC 74LS20
47B	5122 000 09150	IC 74LS74
48B	5122 000 09410	IC 74LS112
50B	2322 151 51002	Resistor 1K MR25
51B	5122 000 11360	Capacitor 100nF 50V
52B	2022 001 00142	Capacitor 33µF 10V
53B	2422 025 89303	Connector MP F088, 2x16
54B	2422 024 88003	Connector FP F088

CONVERSION LIST WMB1

IDENTIFICATION CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
2022 001 00163	5322 124 10057	CAP.33MU 15V
2022 001 00159	5322 124 10019	CAP.25MU 20V
2222 641 70391	4822 122 30091	CAP.390PF 100V
2322 151 51002	5322 116 54549	RESIST.R 1K MR25
2322 151 51781	5322 116 54492	RESIST R178 MR25
-		
2322 151 51783	5322 116 54637	REST.R17K8 MR25
2322 151 53833	5322 116 50483	RESIST 38K3 MR25
2322 151 54641	5322 116 50536	RESIST.R464 MR25
2322 151 54642	5322 116 50484	RES 4K64 0,25W 1%
4322 057 11521	5322 158 14229	COIL 1,5MH
-		
5122 000 05290	4822 130 30594	DIODE BAV10
5122 000 08810	5322 209 85824	IC SE555N
5122 000 09490	5322 209 84954	IC SN74S10N
5122 000 09520	5322 209 85608	IC N8T26AN
5122 000 09820	5322 209 84475	IC N74S04A
5122 000 11820	5322 122 34153	CAP. 100NF 50V
5122 000 09850	5322 209 85728	IC UA79M05AHC
5122 000 10080	5322 209 84167	IC SN74S00N-00
5122 194 25140	5322 216 25542	PCB WMB 1 SLAVE
5122 194 26610	5322 209 14514	MK 4116P-4
9330 907 40112	5322 130 44551	TOR 2N2906A
-		
9331 178 10112	4822 130 34197	DIODE BZX79 C12

CONVERSION LIST WMC1

IDENTIFICATION CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
2322 151 51003	5322 116 54548	RESIST 9.1K MR25
2411 011 07257	5322 208 14116	PIR GM786
2422 024 88003	5322 263 64007	CONNECTOR 2POL
5122 000 09120	5322 209 84823	IC N74LS00A
5122 000 09130	5322 209 85604	IC N74LS11A
-		
5122 000 09140	5322 209 85569	IC SN74LS20N
5122 000 09150	5322 209 84986	IC SN74LS74N-00
5122 000 09240	5322 209 85606	IC N74S85N
5122 000 09250	5322 209 85672	IC N74S138B
5122 000 09410	5322 209 84971	IC 74LS112
-		
5122 000 09490	5322 209 84954	IC SN74S10N
5122 000 09500	5322 209 85669	IC SN74S157N
5122 000 09510	5322 209 85453	IC N74S151B
5122 000 09520	5322 209 85608	IC N8T26AN
5122 000 09600	5322 209 85683	IC N74S174B
-		
5122 000 09650	5322 209 84724	IC SN74S64N
5122 000 09660	5322 209 84995	IC SN74LS08N-00
5122 000 09700	5322 209 84237	IC SN74S112N
5122 000 09820	5322 209 84475	IC N74S04A
5122 000 09960	5322 209 85677	IC N74S38A
-		
5122 000 10040	5322 209 85452	IC N74S86A
5122 000 10080	5322 209 84167	IC SN74S00N-00
5122 000 10090	5322 209 84915	IC N74S11N
5122 000 10100	5322 209 85195	IC SN74S20N
5122 000 10110	5322 209 84183	IC SN74S74N-00
-		
5122 000 10120	5322 209 85676	IC N74LS280A
5122 000 10130	5322 209 85345	IC SN74LS37N-00
5122 000 10600	5322 209 85862	IC SN74LS240N
5122 000 10760	4822 209 80447	IC N74LS393N
5122 000 10780	5322 209 85407	IC N74S02A
-		
5122 000 10800	5322 209 85681	IC N74S08A
5122 000 10810	5322 209 85194	IC SN74S30N
5122 000 10820	5322 209 85679	IC N74S32A
5122 000 10870	5322 209 85673	IC N74S139B
5122 000 10900	5322 209 85451	IC N74S175B
5122 000 11820	5322 122 34153	CAP.100NF 50V
5122 000 11320	5322 242 74379	X-TAL 16MHZ
5122 000 11560	5322 111 94231	RESIST 1K2
5122 194 25150	5322 216 25543	PCB WMC 1 CU